



LIGHTING FOREVER

8 PIN DIP LOW INPUT CURRENT HIGH GAIN SPLIT DARLINGTON PHOTOCOUPLER

6N138 6N139

Features:

- High current transfer ratio – 2000% typical
- High isolation voltage between input and output ($V_{iso}=5000 V_{rms}$)
- Guaranteed performance from 0°C to 70°C
- Pb free and RoHS compliant.
- UL approved (No. 214129)
- VDE approved (No. 132249)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved
- CSA approved (No. 2037145)

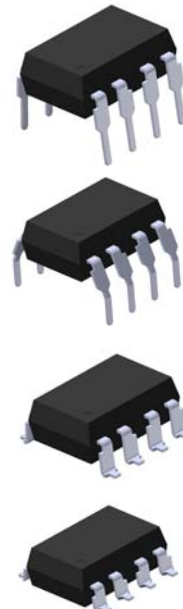
Description

The 6N138 and 6N139 devices each consists of an infrared emitting diode, optically coupled to a high gain split Darlington photo detector. They provide extremely high current transfer ratio between input and output, with access to a base terminal to adjust the gain bandwidth.

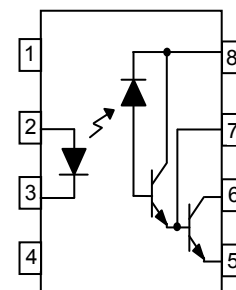
These devices are packaged in an 8-pin DIP package and available in wide-lead spacing and SMD options.

Applications

- Digital logic ground isolation
- RS-232C line receiver
- Low input current line receiver
- Microprocessor bus isolation
- Current loop receiver



Schematic



Pin Configuration

1. No Connection
2. Anode
3. Cathode
4. No Connection
5. Gnd
6. Vout
7. V_B
8. Vcc



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Absolute Maximum Ratings ($T_a=25^{\circ}\text{C}$ unless otherwise specified)

Parameter		Symbol	Rating	Unit	
Input	Forward current	I_F	20	mA	
	Peak forward current (50% duty, 1ms P.W)	I_{FP}	40	mA	
	Peak transient current ($\leq 1 \mu\text{s}$ P.W, 300pps)	I_{Ftrans}	1	A	
	Reverse voltage	V_R	5	V	
	Power dissipation	P_{IN}	45	mW	
Output	Power dissipation	P_O	100	mW	
	Output current	I_O	60	mA	
	Emitter-Base Reverse Voltage	VER	0.5	V	
	Output voltage	6N138	V_O	-0.5 to 7	V
		6N139		-0.5 to 18	V
	Supply voltage	6N138	V_{CC}	-0.5 to 7	V
6N139		-0.5 to 18		V	
Isolation voltage ^{*1}		V_{ISO}	5000	V rms	
Operating temperature		T_{OPR}	-40 ~ +85	$^{\circ}\text{C}$	
Storage temperature		T_{STG}	-55 ~ +125	$^{\circ}\text{C}$	
Soldering temperature ^{*2}		T_{SOL}	260	$^{\circ}\text{C}$	

Notes

*1 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3, 4 are shorted together, and pins 5, 6, 7, 8 are shorted together.

*2 For 10 seconds.



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Electrical Characteristics ($T_a=0$ to 70°C unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Forward voltage	V_F	-	1.3	1.7	V	$I_F = 1.6\text{mA}$
Reverse Voltage	V_R	5.0	-	-	V	$I_R = 10\mu\text{A}$, $T_A=25^\circ\text{C}$
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/ $^\circ\text{C}$	$I_F = 1.6\text{mA}$

Output

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition	
Logic High Output Current	6N139	-	0.01	100	μA	$I_F=0\text{mA}$, $V_O=V_{CC}=18\text{V}$	
	6N138	-	-	250			
Logic Low Supply Current	6N138 6N139	I_{CCL}	-	0.6	1.5	mA	$I_F=1.6\text{mA}$, $V_O=\text{Open}$, $V_{CC}=18\text{V}$
Logic High Supply Current	6N138 6N139	I_{CCH}	-	0.05	10	μA	$I_F=0\text{mA}$, $V_O=\text{Open}$, $V_{CC}=18\text{V}$

Transfer Characteristics ($T_a=0$ to 70°C unless specified otherwise, $V_{CC}=4.5\text{V}$)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition	
Current Transfer Ratio	6N139	CTR	400	2500	-	%	$I_F = 0.5\text{mA}$, $V_O = 0.4\text{V}$, $V_{CC}=4.5\text{V}$
			500	2000	-		$I_F = 1.6\text{mA}$, $V_O = 0.4\text{V}$, $V_{CC}=4.5\text{V}$
	6N138		300	2000	-		
Logic Low Output Voltage	6N139	V_{OL}	-	0.05	0.4	V	$I_F = 0.5\text{mA}$, $I_O = 2\text{mA}$, $V_{CC}=4.5\text{V}$
			-	0.09	0.4		$I_F = 1.6\text{mA}$, $I_O = 8\text{mA}$, $V_{CC}=4.5\text{V}$
			-	0.12	0.4		$I_F = 5\text{mA}$, $I_O = 15\text{mA}$, $V_{CC}=4.5\text{V}$
			-	0.17	0.4		$I_F = 12\text{mA}$, $I_O = 24\text{mA}$, $V_{CC}=4.5\text{V}$
	6N138		-	0.06	0.4		$I_F = 1.6\text{mA}$, $I_O = 4.8\text{mA}$, $V_{CC}=4.5\text{V}$

* Typical values at $T_a = 25^\circ\text{C}$



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Switching Characteristics (T_a=0 to 70°C unless specified otherwise, V_{cc}=5V)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition	
Propagation Delay Time to Logic Low (Fig. 13)	6N139	TPHL	-	5	25	μs	I _F = 0.5mA , R _L =4.7kΩ, T _A =25°C
			-	-	30		I _F = 0.5mA , R _L =4.7kΩ
			-	0.2	1		I _F = 12mA , R _L =270Ω, T _A =25°C
			-	-	2		I _F = 12mA , R _L =270Ω
	6N138	TPHL	-	1.4	10		I _F = 1.6mA , R _L =2.2kΩ, T _A =25°C
			-	-	15		I _F = 1.6mA , R _L =2.2kΩ
Propagation Delay Time to Logic High (Fig. 13)	6N139	TPLH	-	16	60	μs	I _F = 0.5mA , R _L =4.7kΩ, T _A =25°C
			-	-	90		I _F = 0.5mA , R _L =4.7kΩ
			-	1.7	7		I _F = 12mA , R _L =270Ω, T _A =25°C
			-	-	10		I _F = 12mA , R _L =270Ω
	6N138	TPLH	-	8	35		I _F = 1.6mA , R _L =2.2kΩ, T _A =25°C
			-	-	50		I _F = 1.6mA , R _L =2.2kΩ
Common Mode Transient Immunity at Logic High (Fig. 14) ^{*3}	CM _H	1,000	-	-	V/μs	I _F = 0mA , V _{CM} =10Vp-p, R _L =2.2KΩ, T _A =25°C	
Common Mode Transient Immunity at Logic Low (Fig. 14) ^{*3}	CM _L	1,000	-	-	V/μs	I _F = 1.6mA , V _{CM} =10Vp-p, R _L =2.2KΩ, T _A =25°C	

* Typical values at T_a = 25°C

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Typical Performance Curves

Fig.1 LED Forward Current vs. Forward Voltage

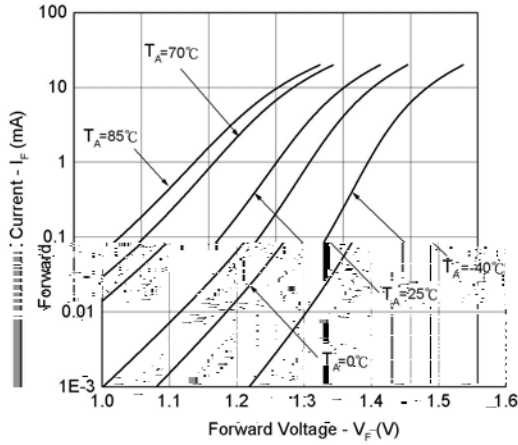


Fig.2 LED Forward Voltage vs. Temperature

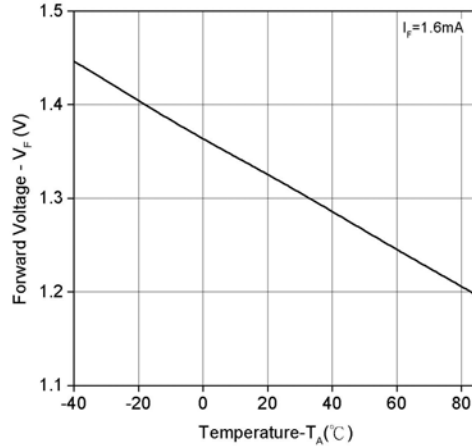


Fig.3 Output Current vs. Output Voltage

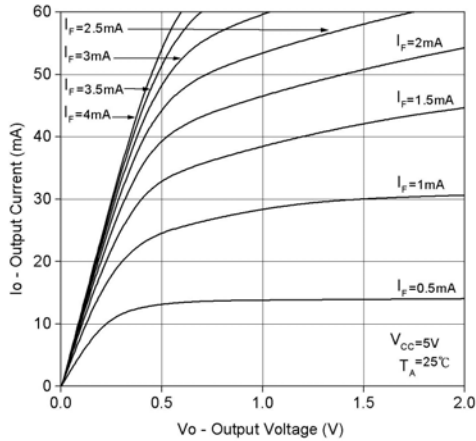


Fig.4 Output Current vs. Input Diode Forward Current

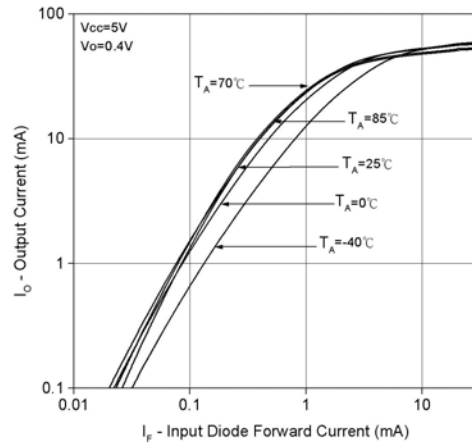


Fig.5 Current Transfer Ratio vs. Forward Current

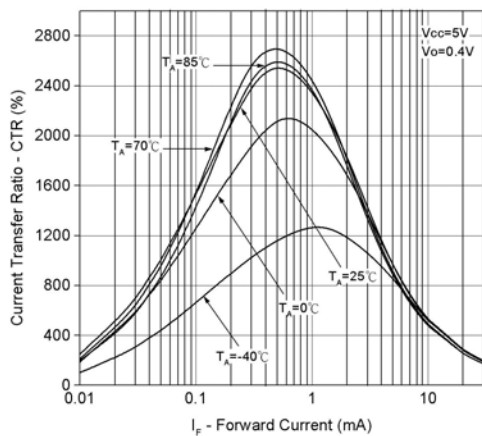
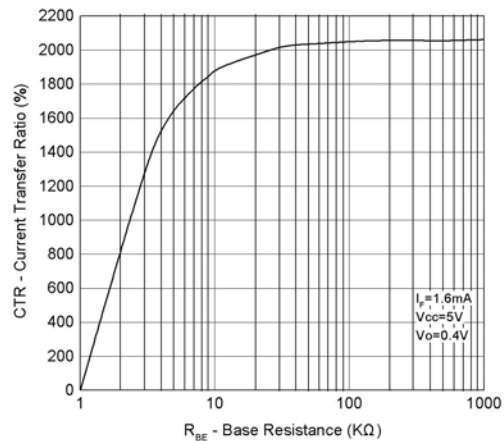


Fig.6 Current Transfer Ratio vs. Base-Emitter Resistance



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Fig.7 Non-saturated Rise and Fall Times vs. Load Resistance

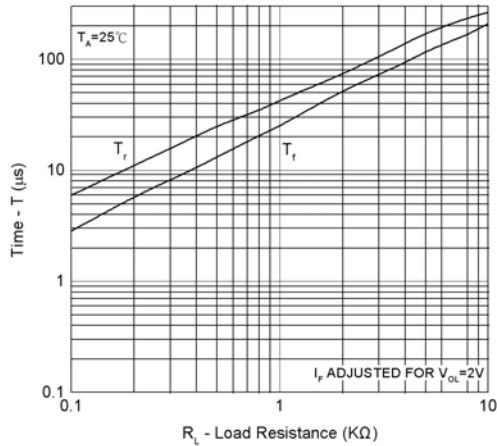


Fig.8 Propagation Delay To Logic Low vs. Base-Emitter Resistance

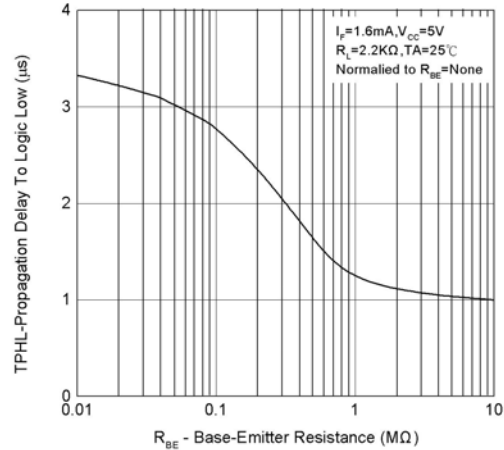


Fig.9 Propagation Delay vs. Input Diode Forward Current

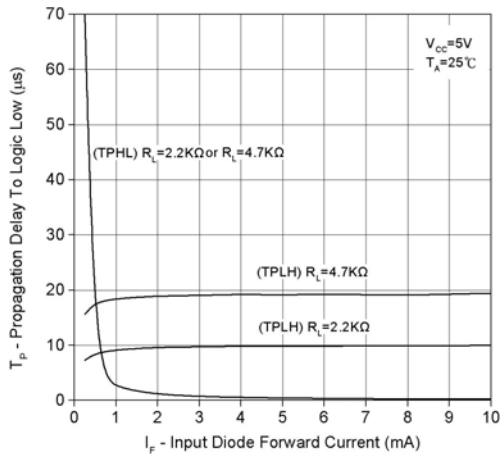


Fig.10 Propagation Delay to Logic Low vs. Pulse Period

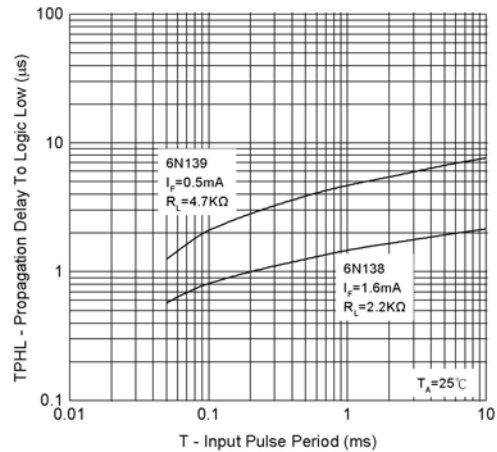


Fig.11 Propagation Delay vs. Temperature

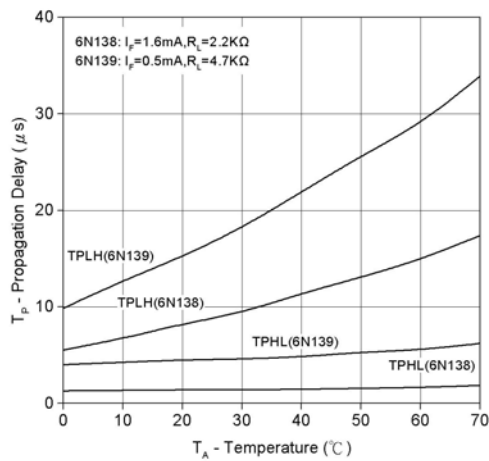
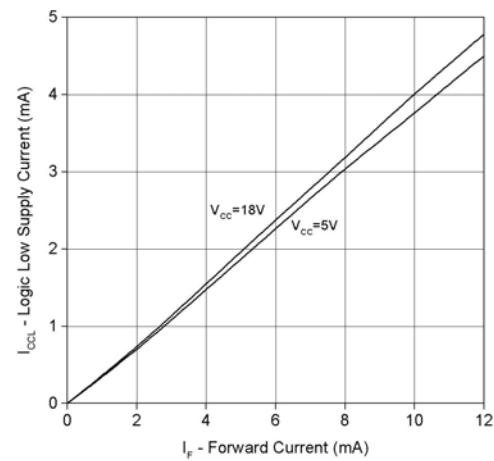


Fig.12 Logic Low Supply Current vs. Input Diode Forward Current



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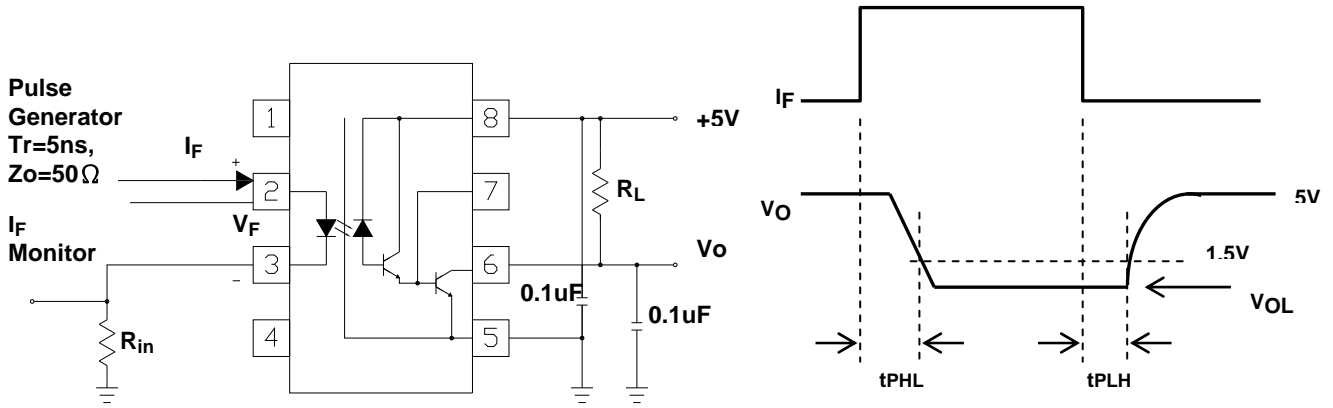


Fig. 13 Switching Time Test Circuit and Waveform

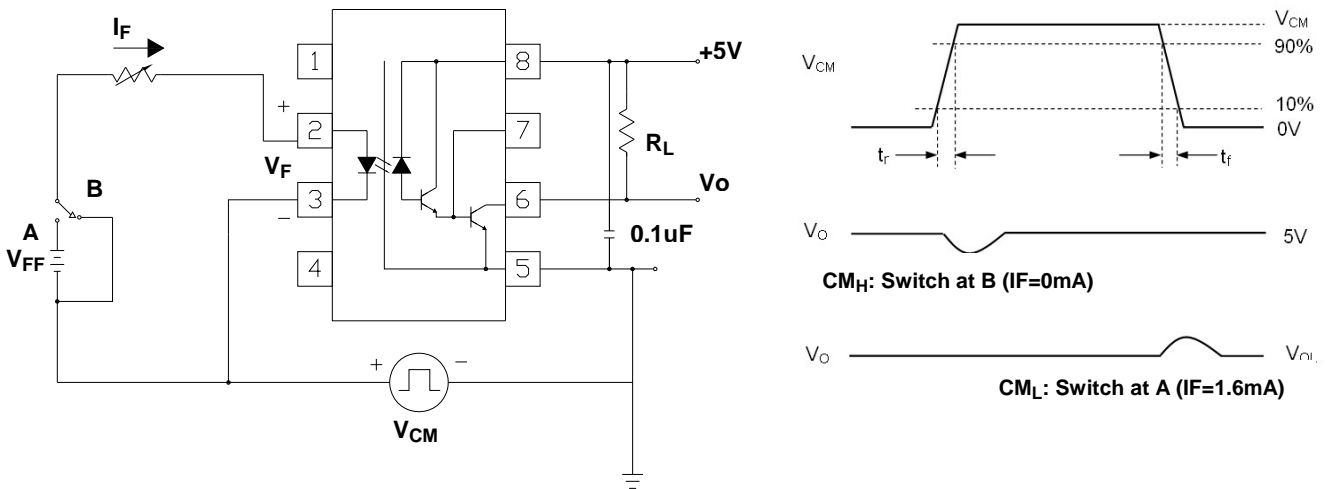


Fig. 14 Common Mode Transient Immunity Test Circuit and Waveform

Note:

*3 Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{cm} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0V$).

Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8V$).



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Order Information

Part Number

6N13XY(Z)-V

Note

- X = Part No. (X = 8 or 9)
- Y = Lead form option (S, S1, M or none)
- Z = Tape and reel option (TA, TB or none).
- V = VDE (optional)

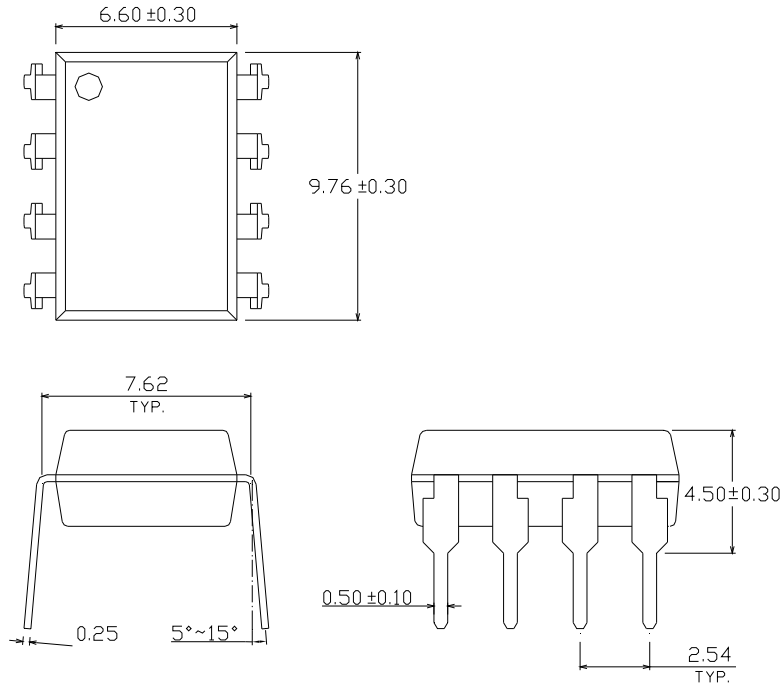
Option	Description	Packing quantity
None	Standard DIP-8	45 units per tube
M	Wide lead bend (0.4 inch spacing)	45 units per tube
S (TA)	Surface mount lead form + TA tape & reel option	1000 units per reel
S (TB)	Surface mount lead form + TB tape & reel option	1000 units per reel
S1 (TA)	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
S1 (TB)	Surface mount lead form (low profile) + TB tape & reel option	1000 units per reel

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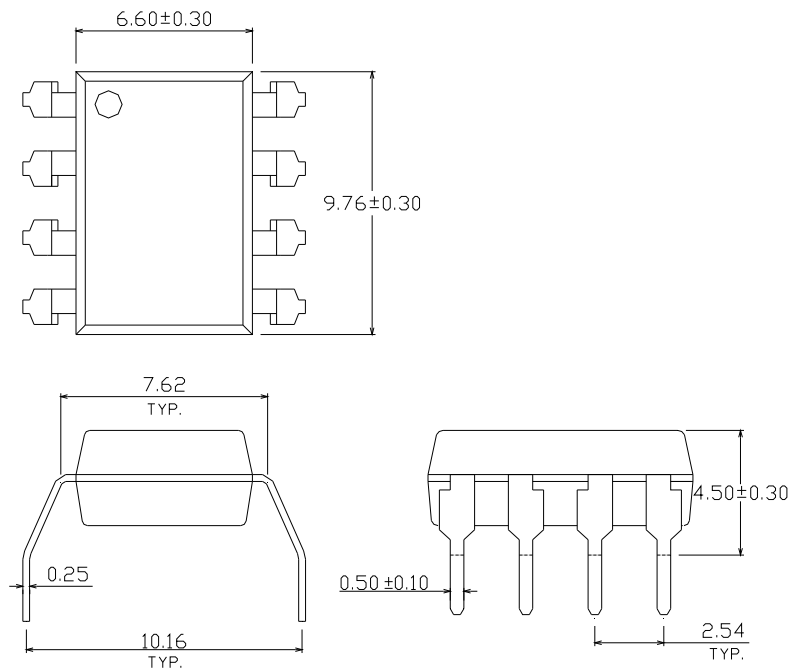
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**Package Drawing
(Dimensions in mm)**

Standard DIP Type



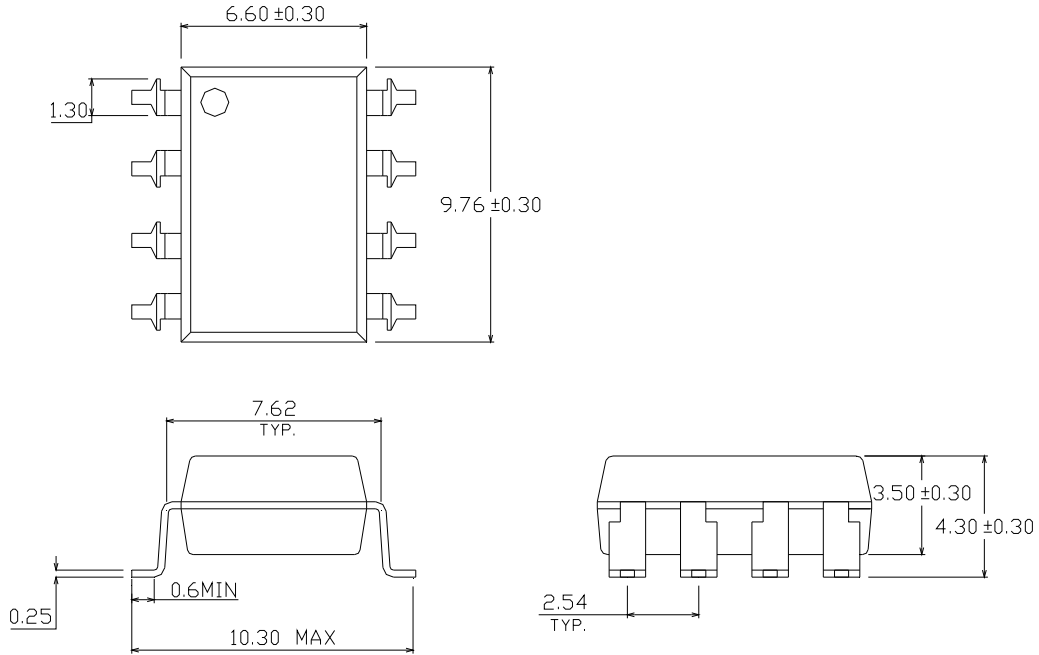
Option M Type



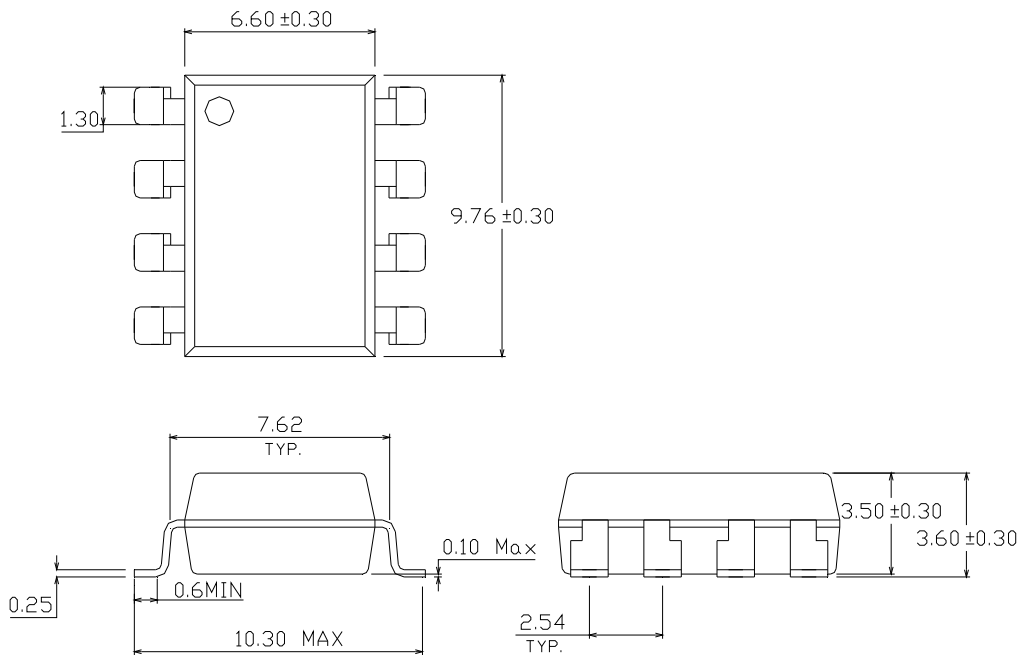
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Option S Type



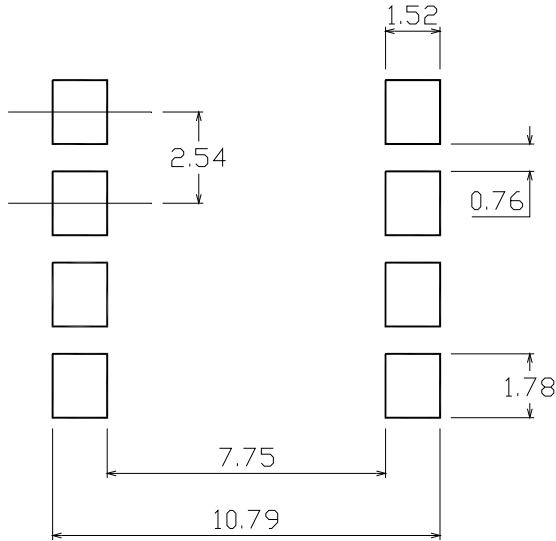
Option S1 Type



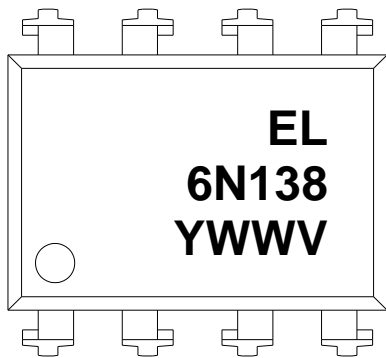
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Recommended pad layout for surface mount leadform



Device Marking



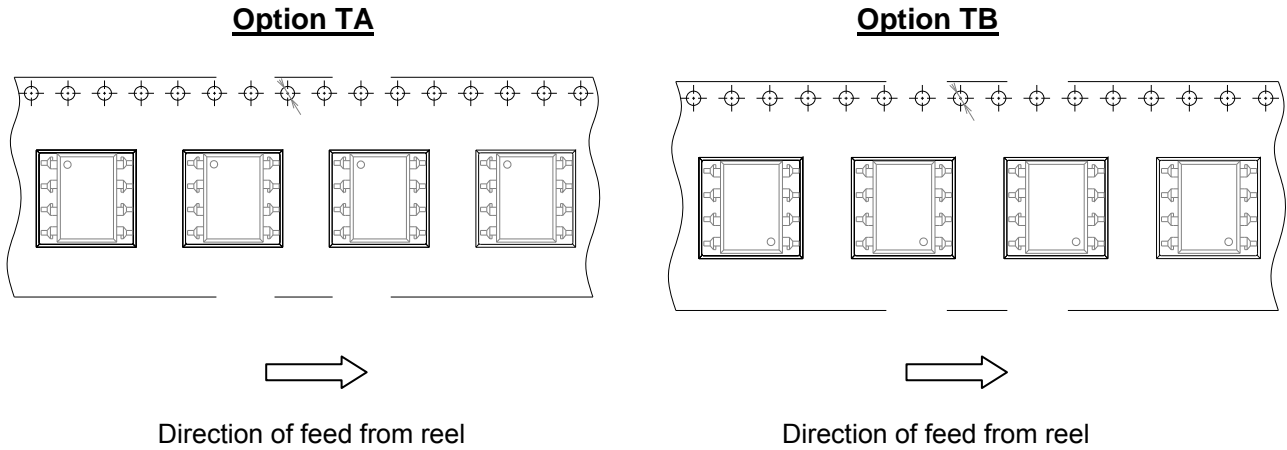
Notes

- 6N138 denotes Device Number
- Y denotes 1 digit Year code
- WW denotes 2 digit Week code
- V denotes VDE (Optional)

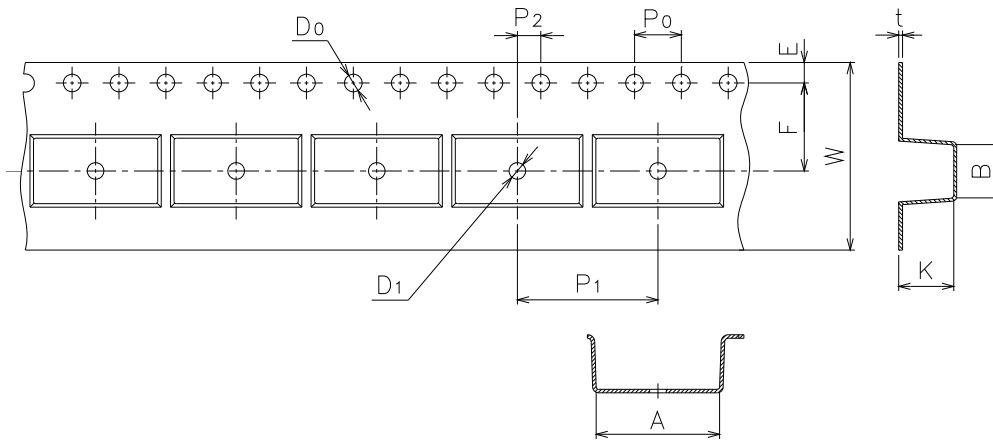
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Tape & Reel Packing Specifications



Tape dimensions

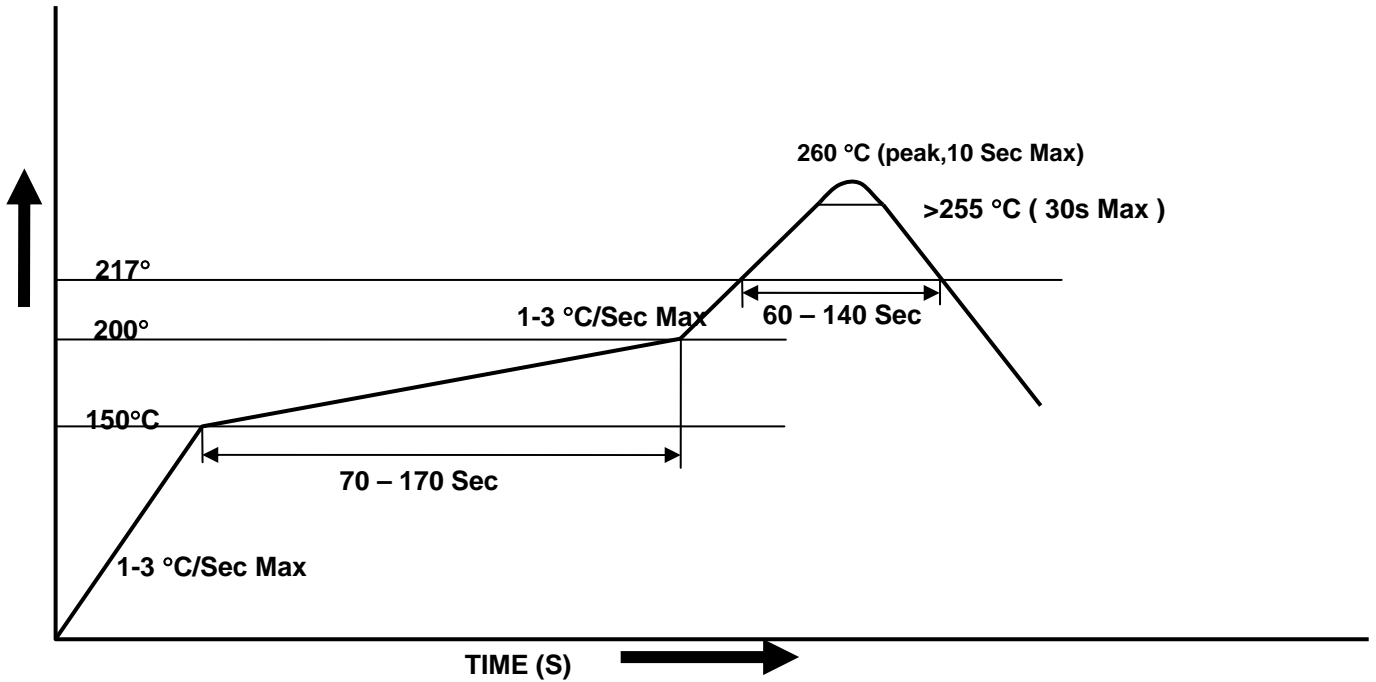


Dimension No.	A	B	Do	D1	E	F
Dimension(mm)	10.4±0.1	10.0±0.1	1.5±0.1	1.5±0.1	1.75±0.1	7.5±0.1
Dimension No.	Po	P1	P2	t	W	K
Dimension(mm)	4.0±0.1	12.0±0.1	2.0±0.1	0.4±0.1	16.0+0.3/ -0.1	4.5±0.1

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Solder Reflow Temperature Profile





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