AT45DB321E

32-Mbit DataFlash (with Extra 1-Mbits), 2.3V Minimum SPI Serial Flash Memory

Features

- Single 2.3V - 3.6V supply
- Serial Peripheral Interface (SPI) compatible
  - Supports SPI modes 0 and 3
  - Supports RapidS™ operation
- Continuous read capability through entire array
  - Up to 85MHz
  - Low-power read option up to 15MHz
  - Clock-to-output time (t_V) of 6ns maximum
- User configurable page size
  - 512 bytes per page
  - 528 bytes per page (default)
  - Page size can be factory pre-configured for 512 bytes
- Two fully independent SRAM data buffers (512/528 bytes)
- Flexible programming options
  - Byte/Page Program (1 to 512/528 bytes) directly into main memory
  - Buffer Write
  - Buffer to Main Memory Page Program
- Flexible erase options
  - Page Erase (512/528 bytes)
  - Block Erase (4KB)
  - Sector Erase (64KB)
  - Chip Erase (32-Mbits)
- Program and Erase Suspend/Resume
- Advanced hardware and software data protection features
  - Individual sector protection
  - Individual sector lockdown to make any sector permanently read-only
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- Hardware and software controlled reset options
- JEDEC Standard Manufacturer and Device ID Read
- Low-power dissipation
  - 400nA Ultra-Deep Power-Down current (typical)
  - 3µA Deep Power-Down current (typical)
  - 25µA Standby current (typical)
  - 11mA Active Read current (typical)
- Endurance: 100,000 program/erase cycles per page minimum
- Data retention: 20 years
- Green (Pb/Halide-free/RoHS compliant) packaging options
  - 8-lead SOIC (0.208" wide)
  - 8-pad Ultra-thin DFN (5 x 6 x 0.6mm)
  - 9-ball Ultra-thin UBGA (6 x 6 x 0.6mm)

Description

The Adesto® AT45DB321E is a 2.3V minimum, serial-interface sequential access Flash memory ideally suited for a wide variety of digital voice, image, program code, and data storage applications. The AT45DB321E also supports the RapidS serial interface for applications requiring very high speed operation. Its 34,603,008 bits of memory are organized as 8,192 pages of 512 bytes or 528 bytes each. In addition to the main memory, the AT45DB321E also contains two SRAM buffers of 512/528 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed. Interleaving between both buffers can dramatically increase a system's ability to write a continuous data stream. In addition, the SRAM buffers can be used as additional system scratch pad memory, and E^2PROM emulation (bit or byte alterability) can be easily handled with a self-contained three step read-modify-write operation.

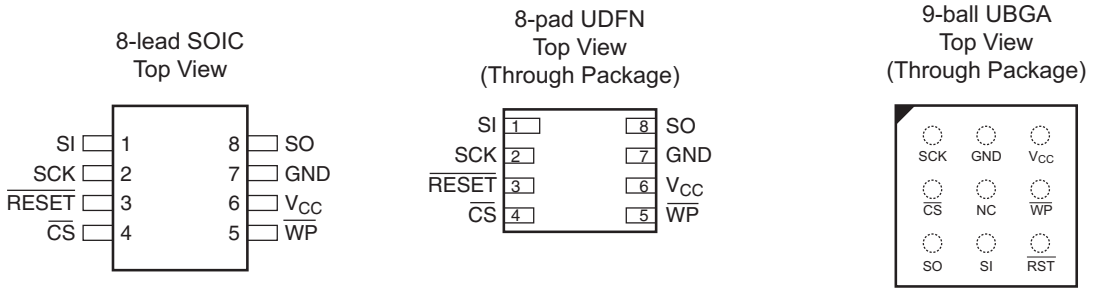
Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the Adesto DataFlash® uses a serial interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates simplified hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage, and low-power are essential.

To allow for simple in-system re-programmability, the AT45DB321E does not require high input voltages for programming. The device operates from a single 2.3V to 3.6V power supply for the erase and program and read operations. The AT45DB321E is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK).

All programming and erase cycles are self-timed.

1. Pin Configurations and Pinouts

Figure 1-1. Pinouts



Note: 1. The metal pad on the bottom of the UDFN package is not internally connected to a voltage potential. This pad can be a “no connect” or connected to GND.

18. Electrical Specifications

18.1 Absolute Maximum Ratings*

Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (except V_{CC} but including NC pins) with Respect to Ground	-0.6V to V_{CC} + 0.6V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. The “Absolute Maximum Ratings” are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

18.2 DC and AC Operating Range

		AT45DB321E 2.3V
Operating Temperature (Case)	Industrial	-40°C to 85°C
V_{CC} Power Supply		2.3V to 3.6V

18.3 DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{UDPD}	Ultra-Deep Power-Down Current	All inputs at 0V or V_{CC}		0.4	1	µA
I_{DPD}	Deep Power-Down Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH} All inputs at CMOS levels		5	12	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH} All inputs at CMOS levels		25	50	µA
I_{CC1}	Active Current, Low Power Read (01h) Operation	f = 1MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		6	9	mA
		f = 15MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		7	11	mA
I_{CC2} (1)(2)	Active Current, Read Operation	f = 50MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		12	17	mA
		f = 85MHz; I_{OUT} = 0mA; V_{CC} = 3.6V		16	22	mA
I_{CC3}	Active Current, Program Operation	$\overline{CS}$=V_{CC}		12	18	mA
I_{CC4}	Active Current, Erase Operation	$\overline{CS}$=V_{CC}		12	18	mA
I_{LI}	Input Load Current	All inputs at CMOS levels			1	µA
I_{LO}	Output Leakage Current	All inputs at CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.6	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{CC} - 0.2V			V

Notes: 1. Typical values measured at 3.0V at 25°C.
2. I_{CC2} during a Buffer Read is 20mA maximum @ 20MHz.

18.4 AC Characteristics

Symbol	Parameter		Min	Max	Units
f_{SCK}	SCK Frequency			70	MHz
f_{CAR1}	SCK Frequency for Continuous Read (0x0B)			85	MHz
f_{CAR2}	SCK Frequency for Continuous Read (0x03) (Low Frequency)			50	MHz
f_{CAR3}	SCK Frequency for Continuous Read (Low Power Mode – 01h Opcode)			15	MHz
f_{CAR4}	SCK Frequency for Continuous Read (0x1B)			104	MHz
t_{WH}	SCK High Time		4		ns
t_{WL}	SCK Low Time		4		ns
t_{SCKR}[1]	SCK Rise Time, Peak-to-peak		0.1		V/ns
t_{SCKF}[1]	SCK Fall Time, Peak-to-peak		0.1		V/ns
t_{CS}	Minimum $\overline{CS}$ High Time		20		ns
t_{CSS}	$\overline{CS}$ Setup Time		5		ns
t_{CSH}	$\overline{CS}$ Hold Time		5		ns
t_{SU}	Data In Setup Time		2		ns
t_{H}	Data In Hold Time		1		ns
t_{HO}	Output Hold Time		0		ns
t_{DIS}	Output Disable Time			6	ns
t_{V}	Output Valid			7	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1	µs
t_{LOCK}	Freeze Sector Lockdown Time (from $\overline{CS}$ High)			100	µs
t_{EUDPD}	$\overline{CS}$ High to Ultra-Deep Power-Down			4	µs
t_{CSLU}	Minimum $\overline{CS}$ Low Time to Exit Ultra-Deep Power-Down		20		ns
t_{XUDPD}	Exit Ultra-Deep Power-Down Time			180	µs
t_{EDPD}	$\overline{CS}$ High to Deep Power-Down			2	µs
t_{RDPD}	Resume from Deep Power-Down Time			35	µs
t_{XFR}	Page to Buffer Transfer Time			200	µs
t_{COMP}	Page to Buffer Compare Time			200	µs
t_{RST}	$\overline{RESET}$ Pulse Width		10		µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs
t_{SWRST}	Software Reset Time			35	µs

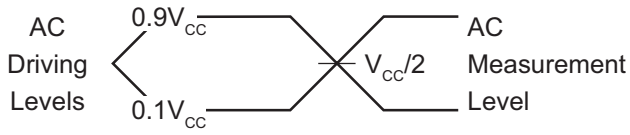
Note: 1. Values are based on device characterization, not 100% tested in production.

18.5 Program and Erase Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{EP}	Page Erase and Programming Time (512/528 bytes)			17	35	ms
t_{P}	Page Programming Time			3	4	ms
t_{BP}	Byte Programming Time			8		µs
t_{PE}	Page Erase Time			12	35	ms
t_{BE}	Block Erase Time			45	100	ms
t_{SE}	Sector Erase Time			0.7	1.4	s
t_{CE}	Chip Erase Time			45	80	s
t_{SUSP}	Suspend Time	Program		10	15	µs
		Erase		20	30	
t_{RES}	Resume Time	Program		10	15	µs
		Erase		20	30	
t_{OTPP}	OTP Security Register Program Time			200	500	µs

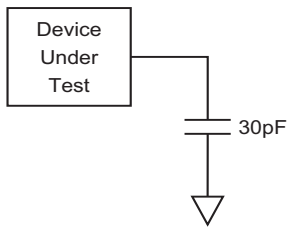
Notes: 1. Values are based on device characterization, not 100% tested in production.
2. Not 100% tested (value guaranteed by design and characterization).

19. Input Test Waveforms and Measurement Levels



t_R, t_F < 2ns (10% to 90%)

20. Output Test Load

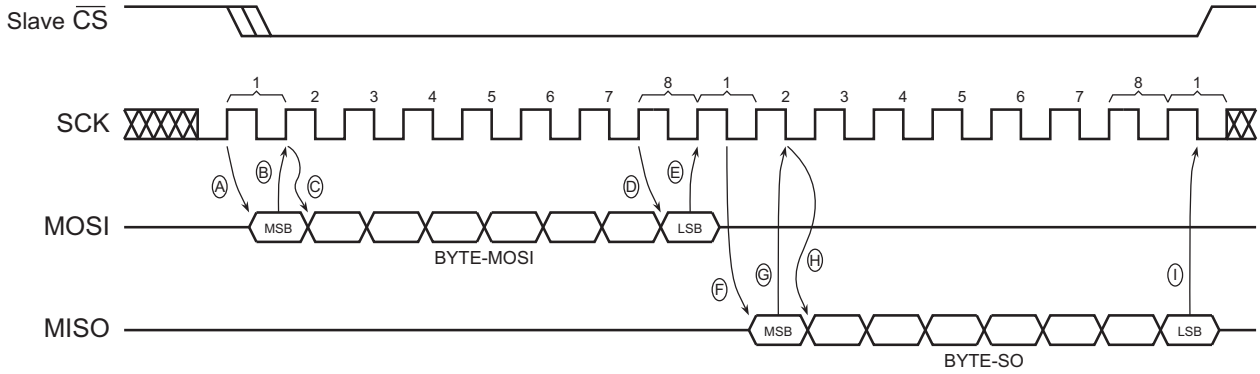


21. Utilizing the RapidS Function

To take advantage of the RapidS function's ability to operate at higher clock frequencies, a full clock cycle must be used to transmit data back and forth across the serial bus. The DataFlash is designed to always clock its data out on the falling edge of the SCK signal and clock data in on the rising edge of SCK.

For full clock cycle operation to be achieved, when the DataFlash is clocking data out on the falling edge of SCK, the host controller should wait until the next falling edge of SCK to latch the data in. Similarly, the host controller should clock its data out on the rising edge of SCK in order to give the DataFlash a full clock cycle to latch the incoming data in on the next rising edge of SCK.

Figure 21-1. RapidS Mode



MOSI = Master Out, Slave In
MISO = Master In, Slave Out
The Master is the host controller and the Slave is the DataFlash.

The Master always clocks data out on the rising edge of SCK and always clocks data in on the falling edge of SCK.
The Slave always clocks data out on the falling edge of SCK and always clocks data in on the rising edge of SCK.

A. Master clocks out first bit of BYTE-MOSI on the rising edge of SCK
B. Slave clocks in first bit of BYTE-MOSI on the next rising edge of SCK
C. Master clocks out second bit of BYTE-MOSI on the same rising edge of SCK
D. Last bit of BYTE-MOSI is clocked out from the Master
E. Last bit of BYTE-MOSI is clocked into the slave
F. Slave clocks out first bit of BYTE-SO
G. Master clocks in first bit of BYTE-SO
H. Slave clocks out second bit of BYTE-SO
I. Master clocks in last bit of BYTE-SO

Figure 21-2. Command Sequence for Read/Write Operations for Page Size 512 bytes
(Except Status Register Read, Manufacturer and Device ID Read)

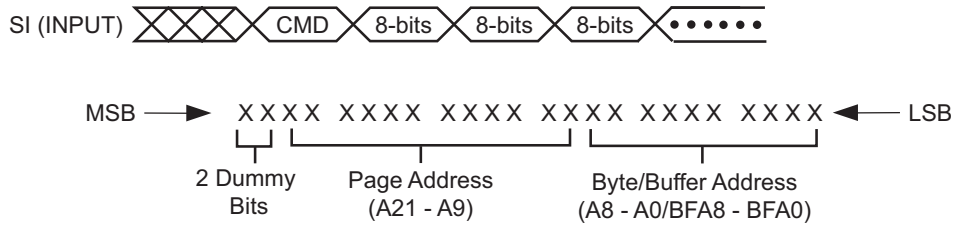
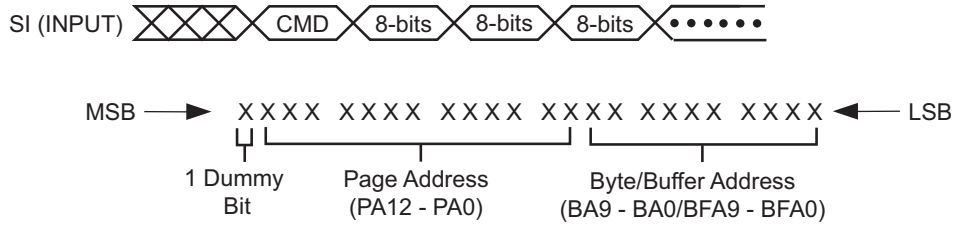


Figure 21-3. Command Sequence for Read/Write Operations for Page Size 528 bytes
(Except Status Register Read, Manufacturer and Device ID Read)



22. AC Waveforms

Four different timing waveforms are shown in Figure 22-1 through Figure 22-4. Waveform 1 shows the SCK signal being low when $\overline{CS}$ makes a high-to-low transition and Waveform 2 shows the SCK signal being high when $\overline{CS}$ makes a high-to-low transition. In both cases, output SO becomes valid while the SCK signal is still low (SCK low time is specified as t_{WL}). Timing Waveforms 1 and 2 conform to RapidS serial interface but for frequencies up to 85MHz. Waveforms 1 and 2 are compatible with SPI Mode 0 and SPI Mode 3, respectively.

Waveform 3 and 4 illustrate general timing diagram for RapidS serial interface. These are similar to Waveform 1 and 2, except that output SO is not restricted to become valid during the t_{WL} period. These timing waveforms are valid over the full frequency range (maximum frequency = 85MHz) of the RapidS serial case.

Figure 22-1. Waveform 1 = SPI Mode 0 Compatible

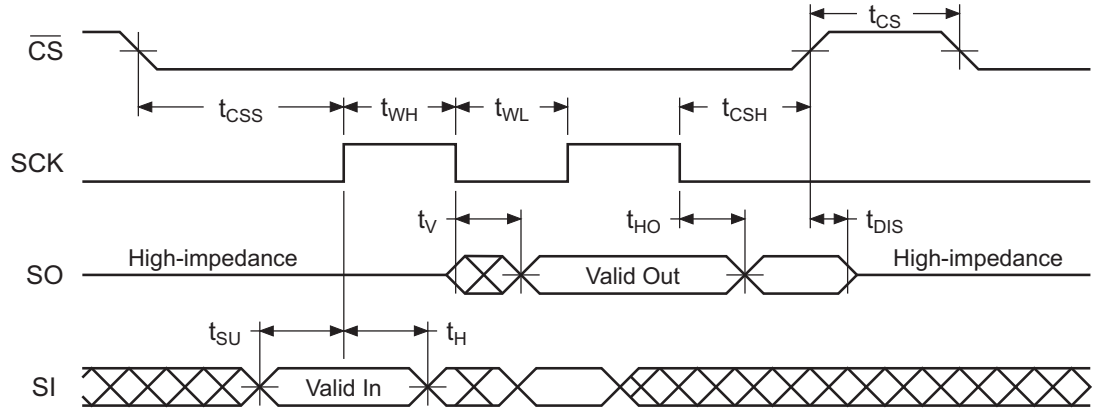


Figure 22-2. Waveform 2 = SPI Mode 3 Compatible

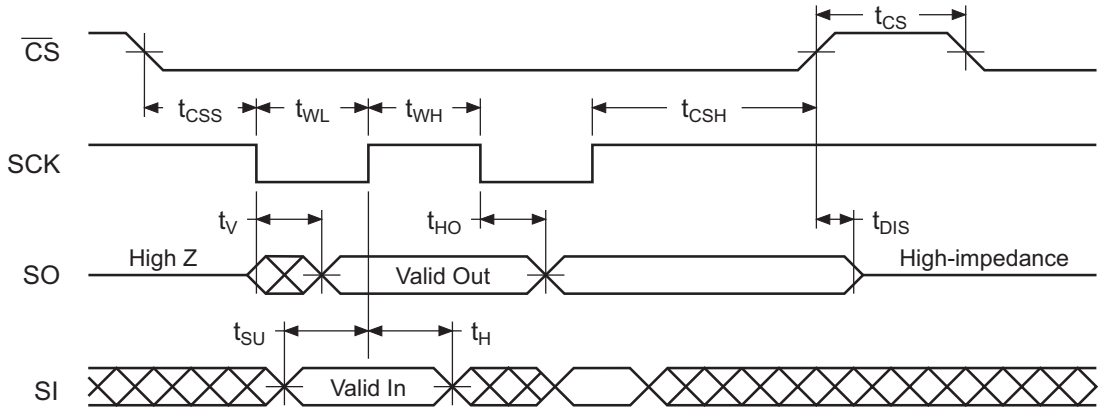


Figure 22-3. Waveform 3 = RapidS Mode 0

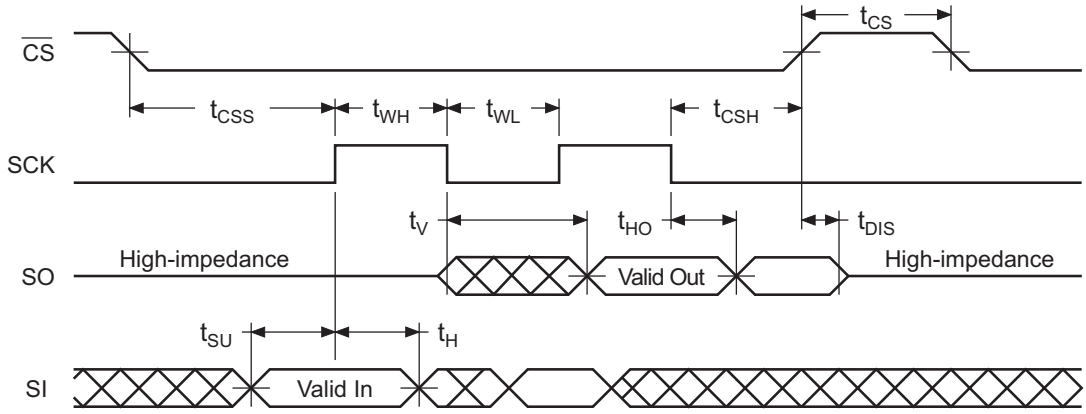
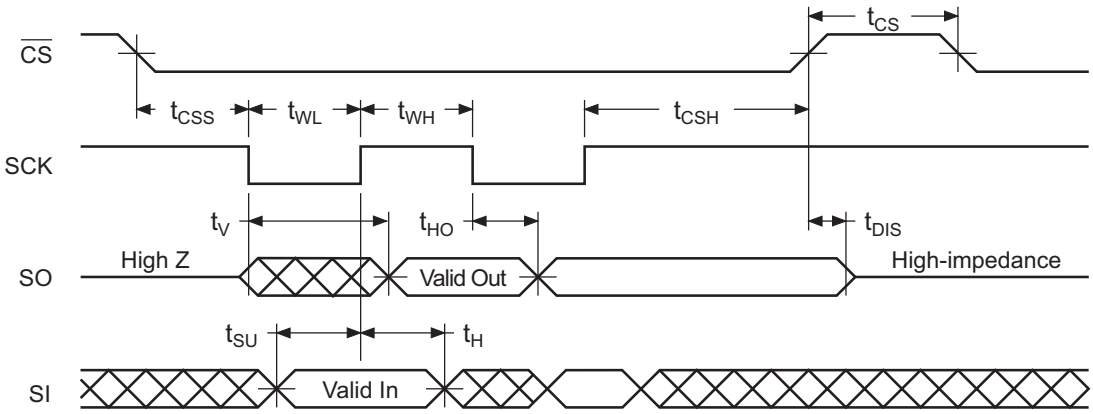


Figure 22-4. Waveform 4 = RapidS Mode 3



23. Write Operations

The following block diagram and waveforms illustrate the various write sequences available.

Figure 23-1. Block Diagram

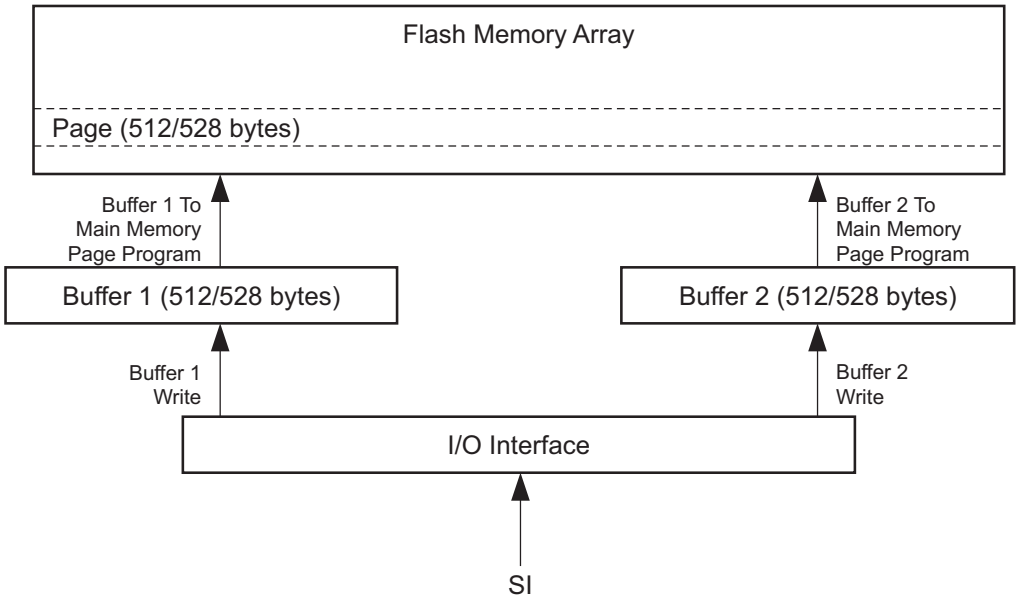


Figure 23-2. Buffer Write

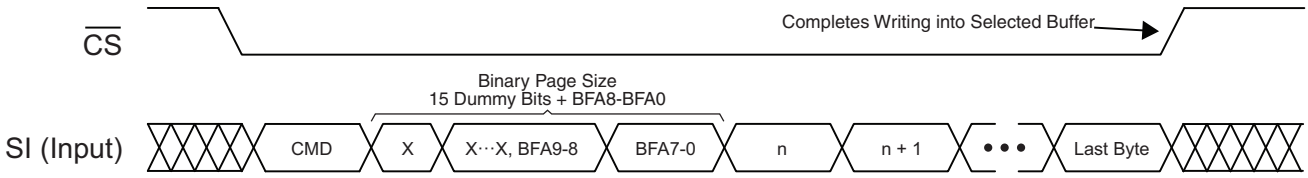
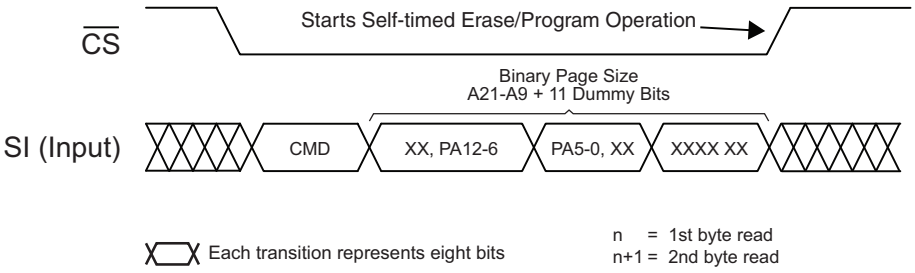


Figure 23-3. Buffer to Main Memory Page Program



24. Read Operations

The following block diagram and waveforms illustrate the various read sequences available.

Figure 24-1. Block Diagram

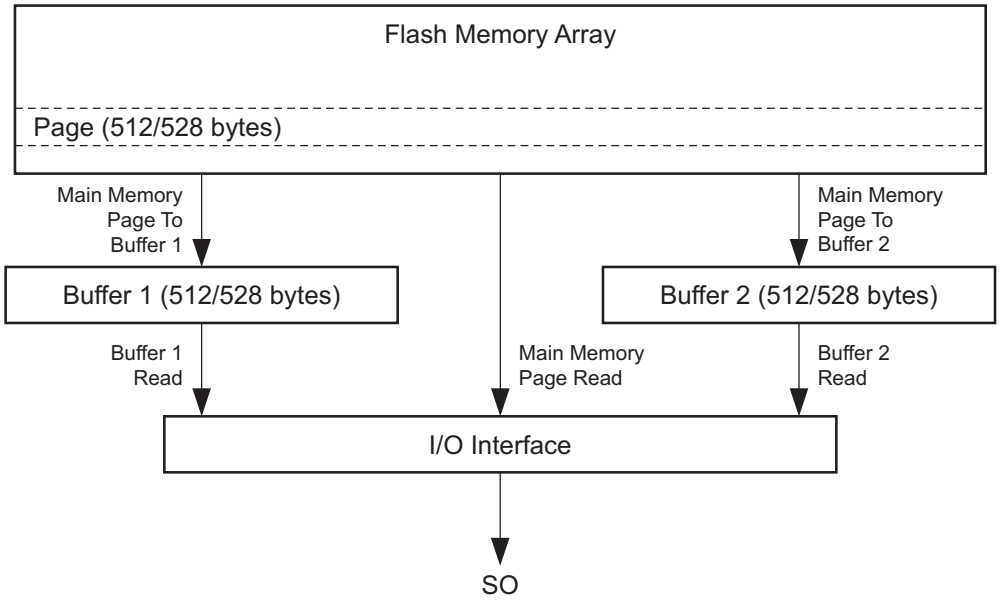


Figure 24-2. Main Memory Page Read

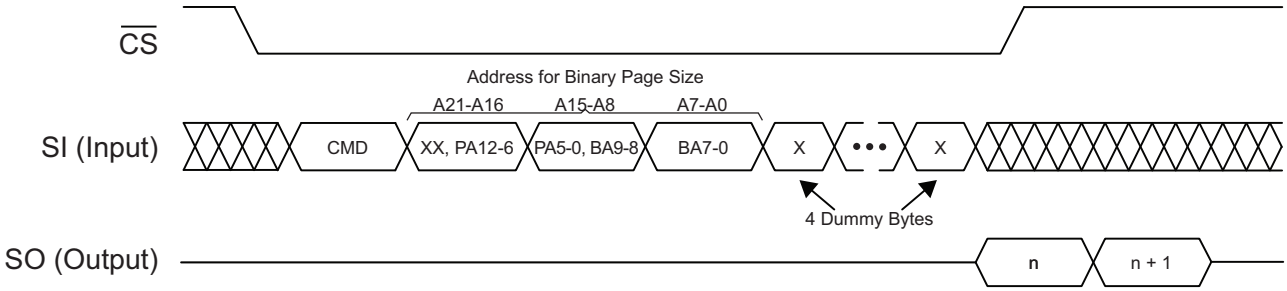


Figure 24-3. Main Memory Page to Buffer Transfer

Data From the selected Flash Page is read into either SRAM Buffer

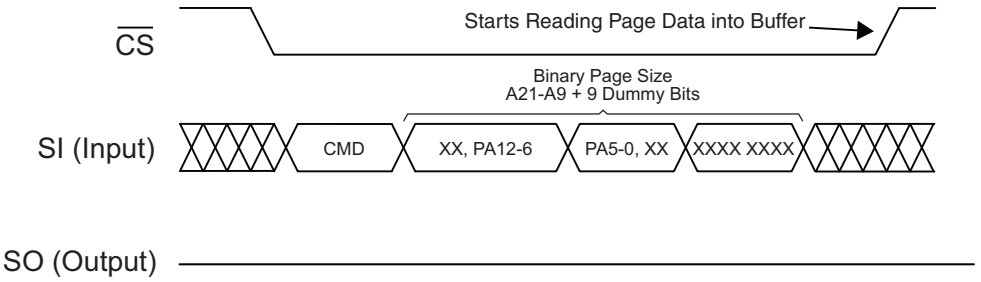
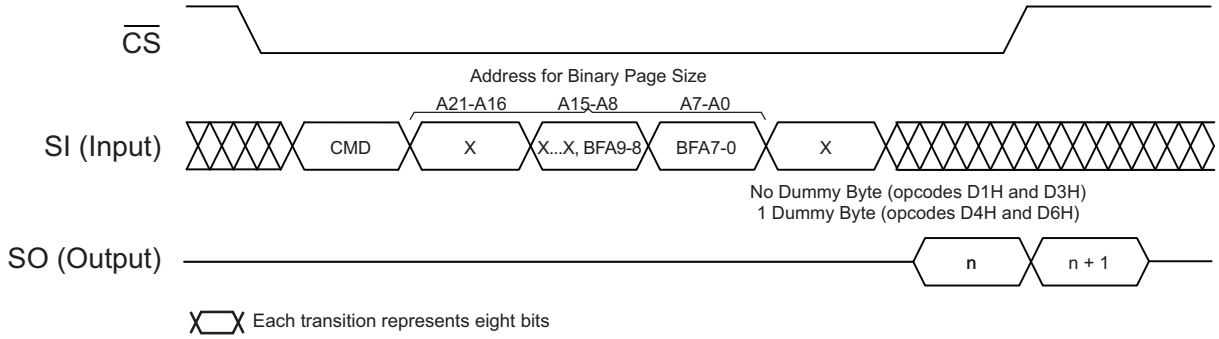


Figure 24-4. Buffer Read



25. Detailed Bit-level Read Waveforms: RapidS Mode 0/Mode 3

Figure 25-1. Continuous Array Read (Legacy Opcode E8h)

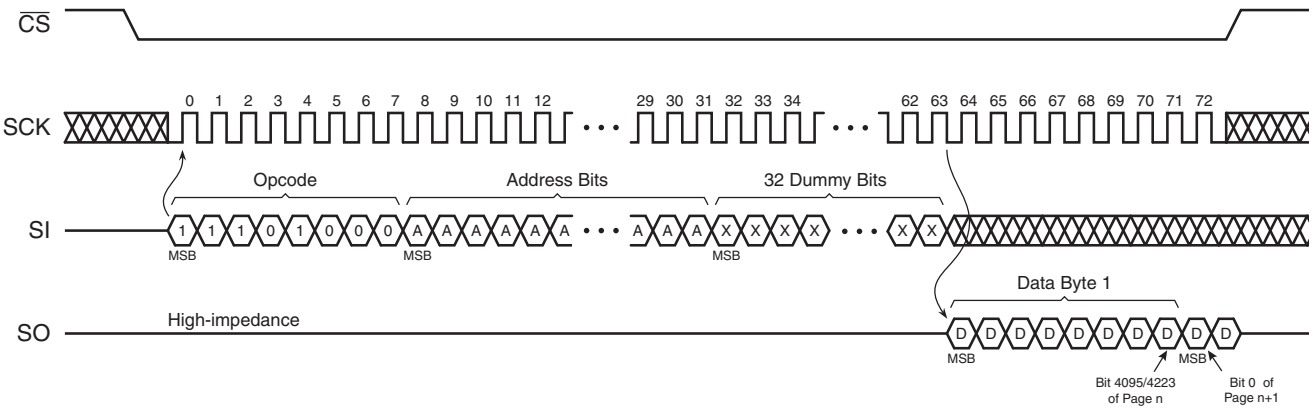


Figure 25-2. Continuous Array Read (Opcode 0Bh)

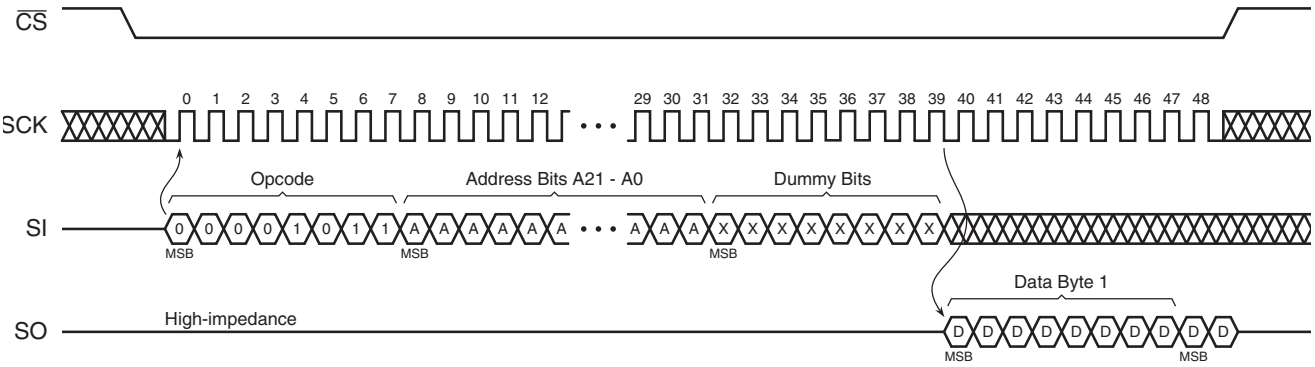


Figure 25-3. Continuous Array Read (Opcode 01h or 03h)

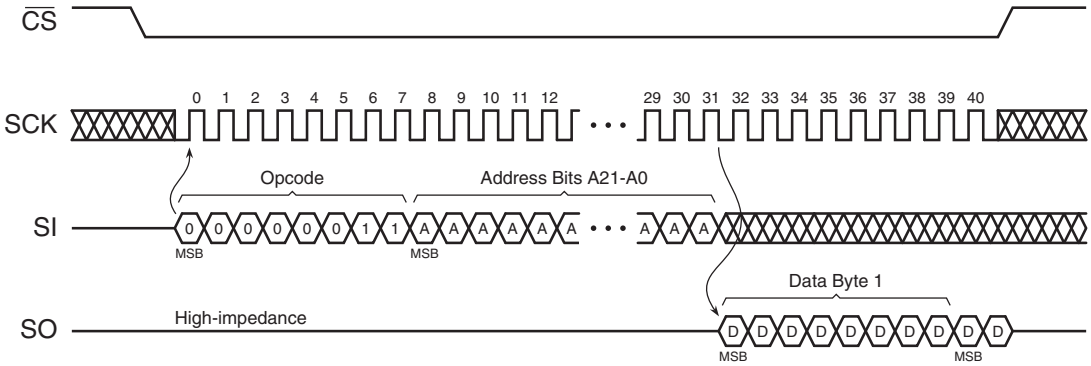


Figure 25-4. Main Memory Page Read (Opcode D2h)

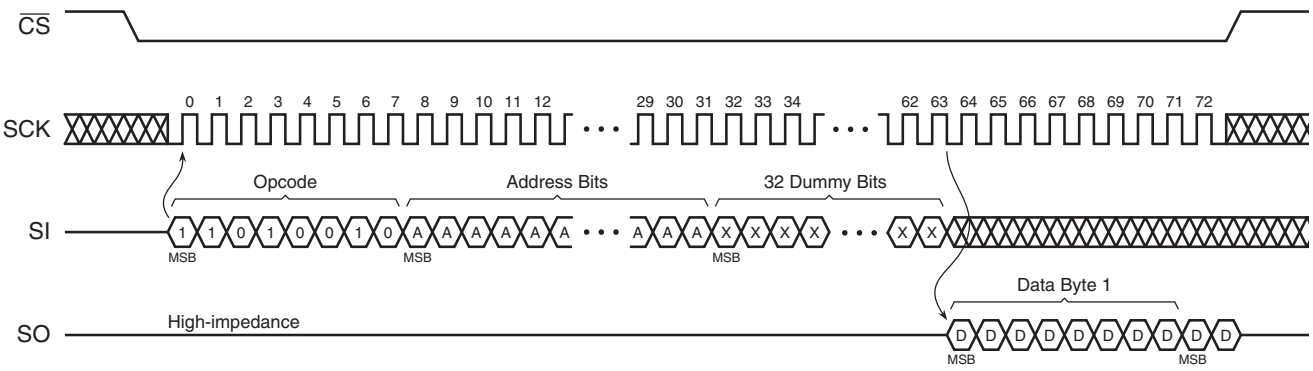


Figure 25-5. Buffer Read (Opcode D4h or D6h)

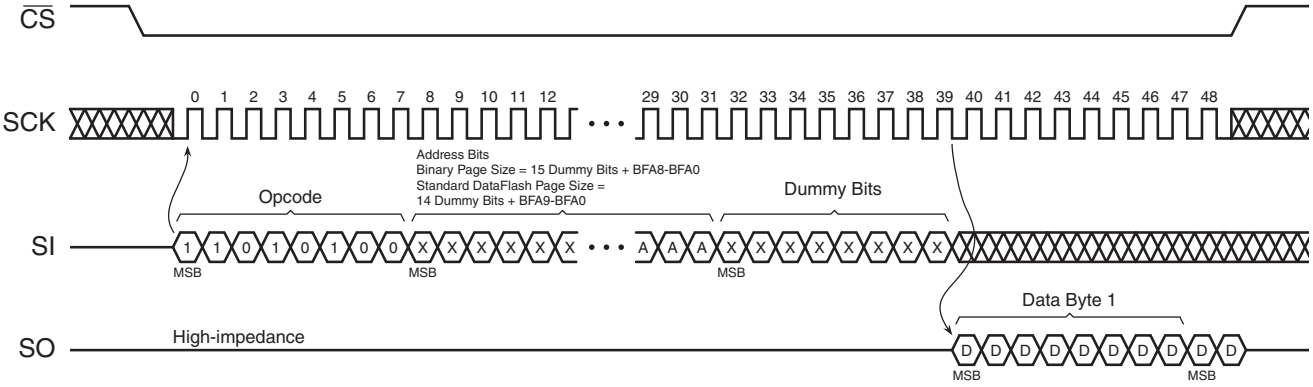


Figure 25-6. Buffer Read – Low Frequency (Opcode D1h or D3h)

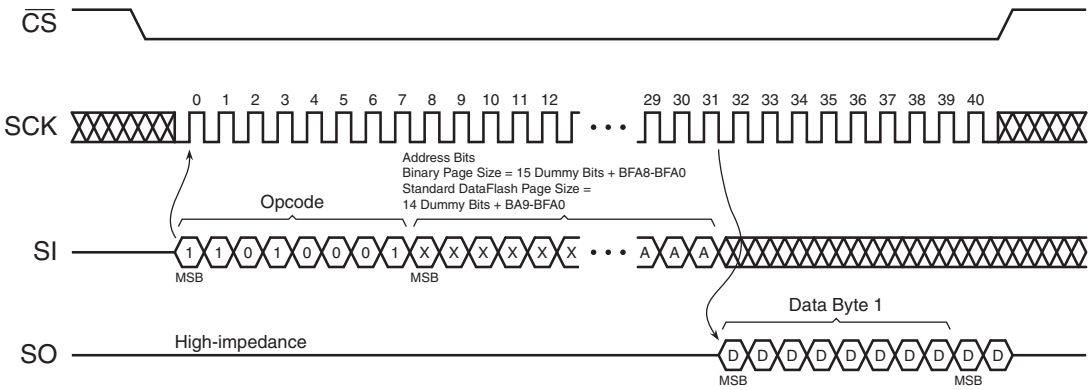


Figure 25-7. Read Sector Protection Register (Opcode 32h)

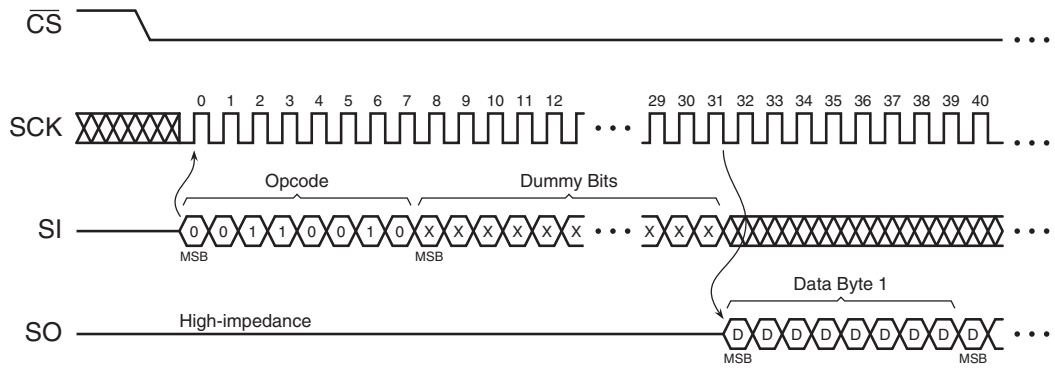


Figure 25-8. Read Sector Lockdown Register (Opcode 35h)

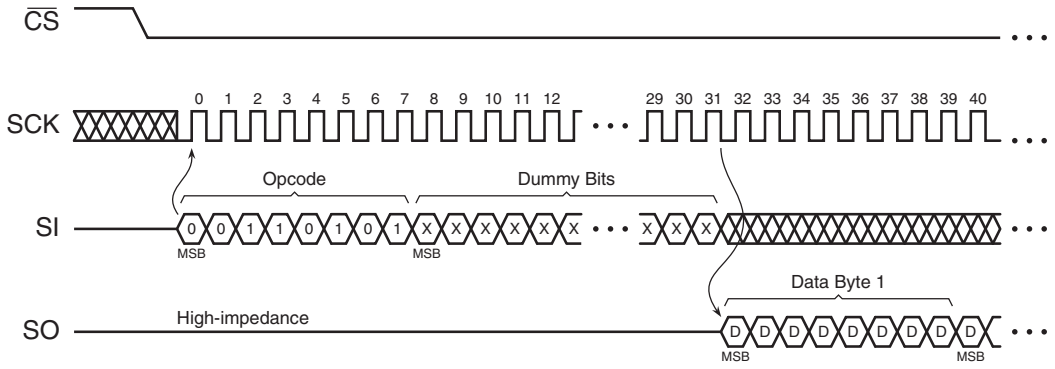


Figure 25-9. Read Security Register (Opcode 77h)

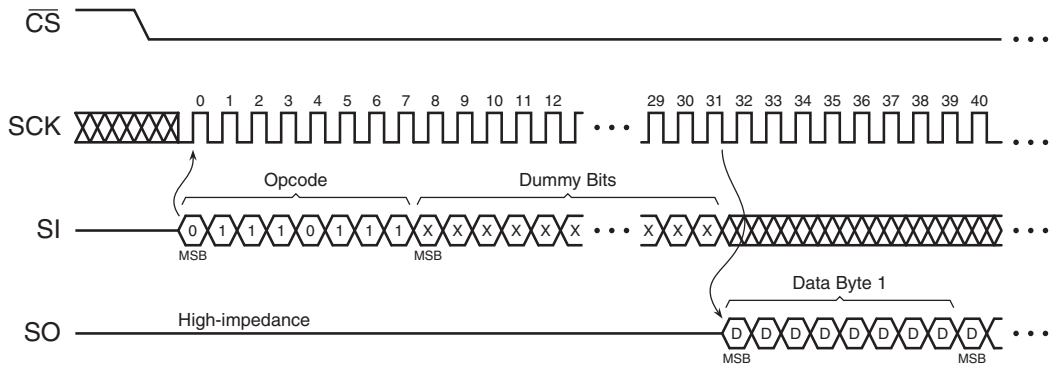


Figure 25-10. Status Register Read (Opcode D7h)

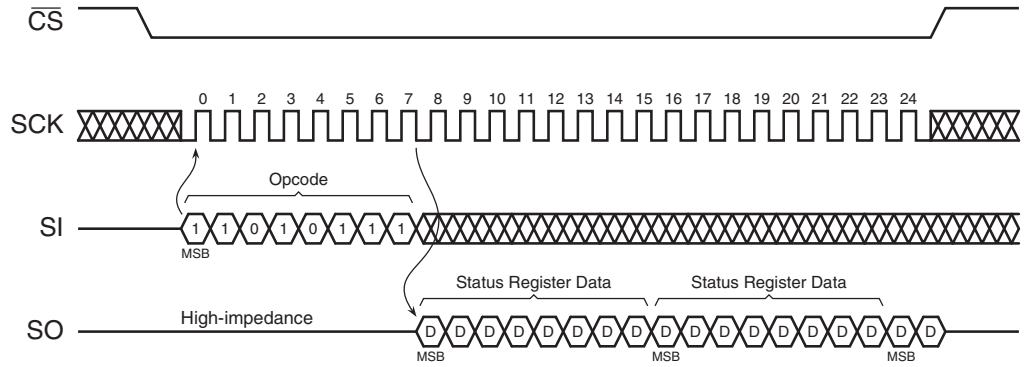


Figure 25-11. Manufacturer and Device Read (Opcode 9Fh)

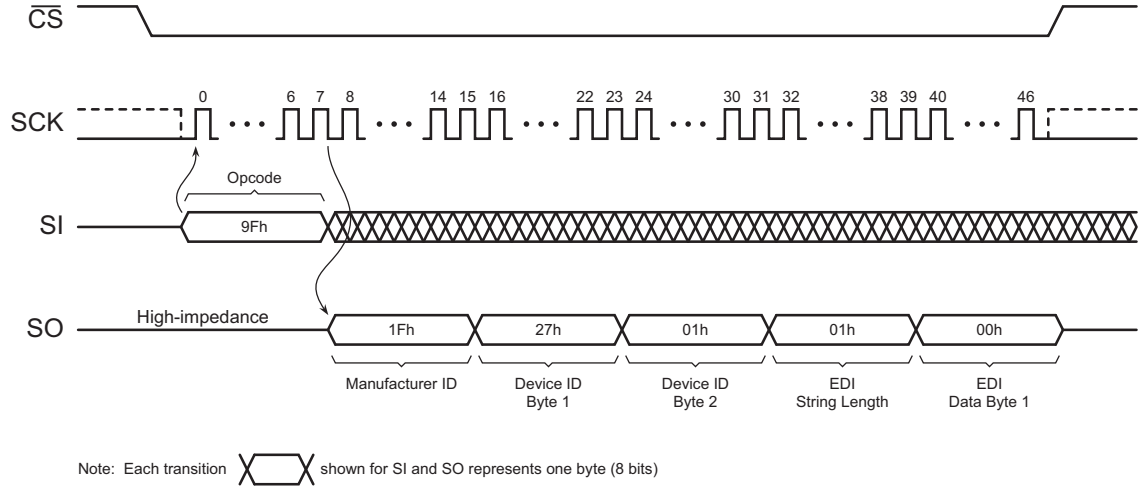
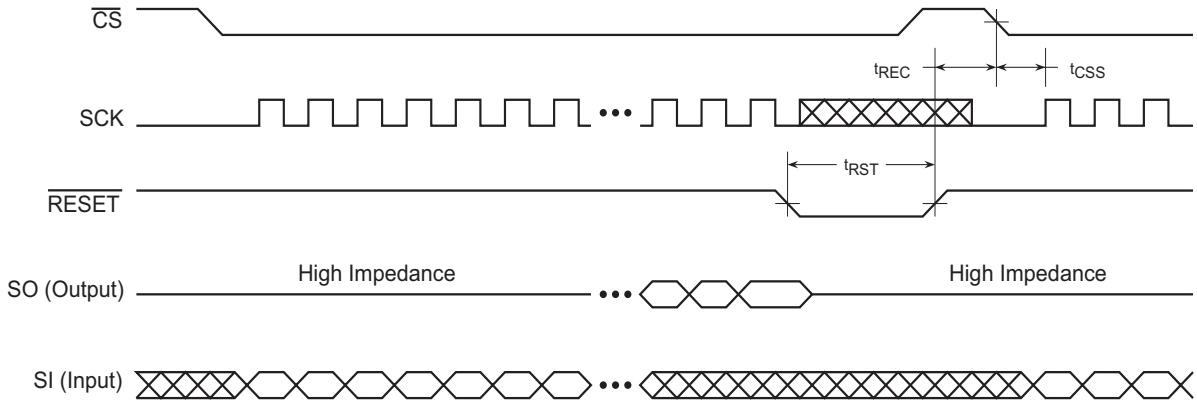


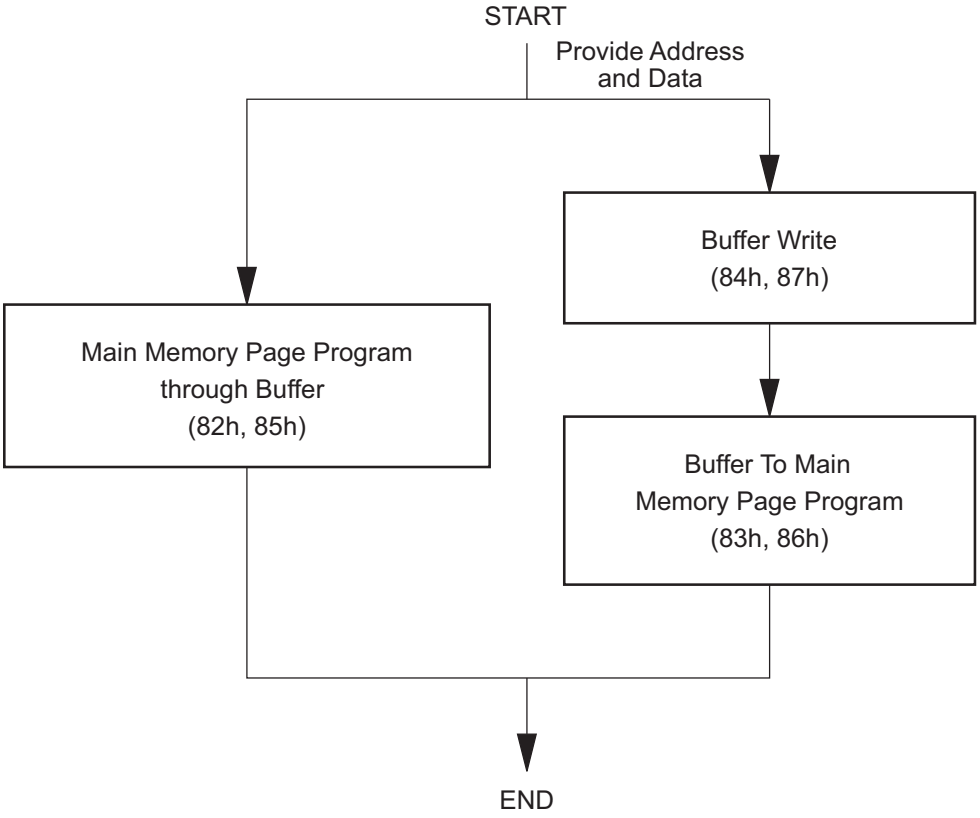
Figure 25-12.Reset Timing



Note: 1. The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

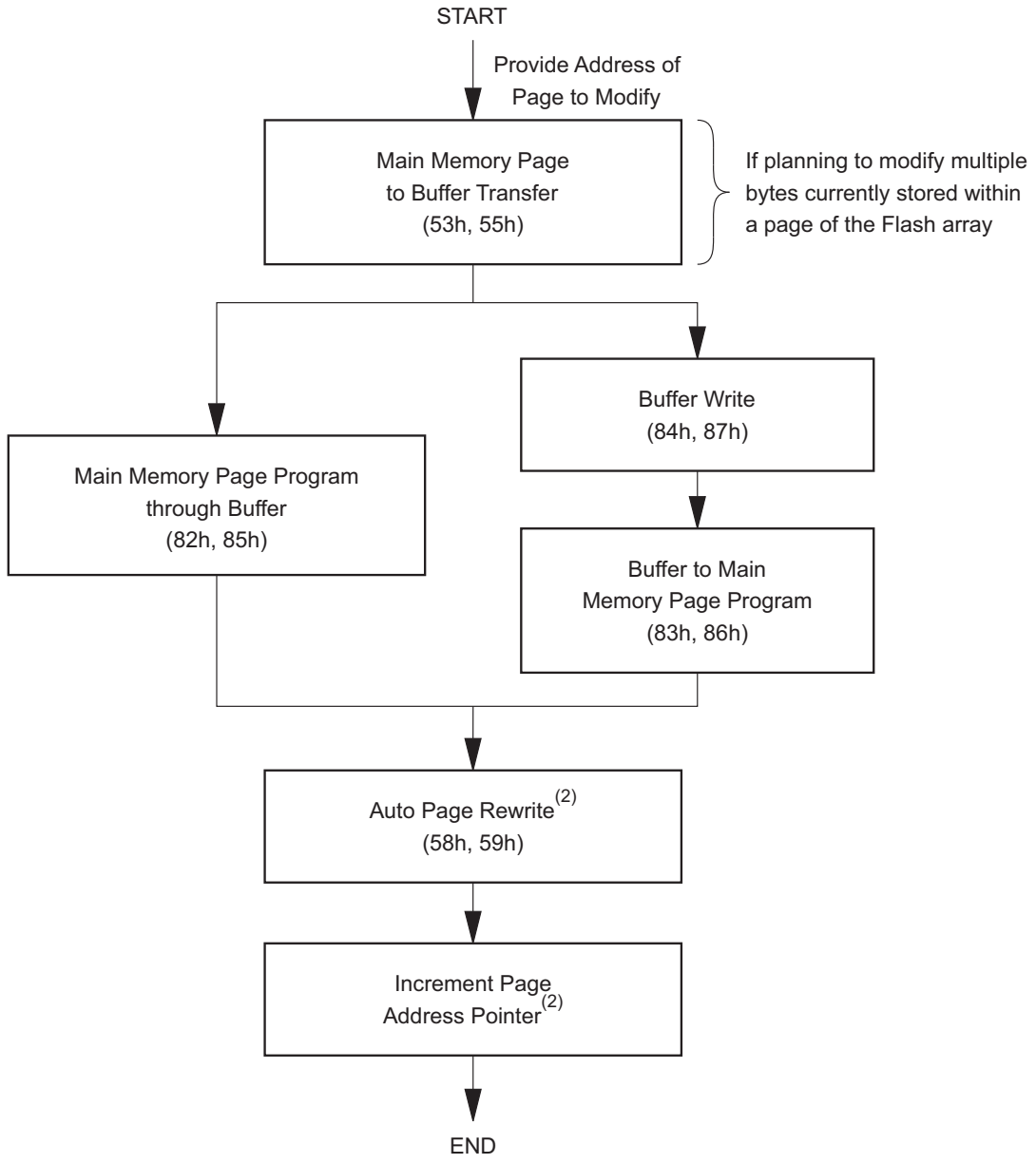
26. Auto Page Rewrite Flowchart

Figure 26-1. Algorithm for Programming or Re-programming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page
2. A page can be written using either a Main Memory Page Program operation or a buffer write operation followed by a buffer to Main Memory Page Program operation
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array

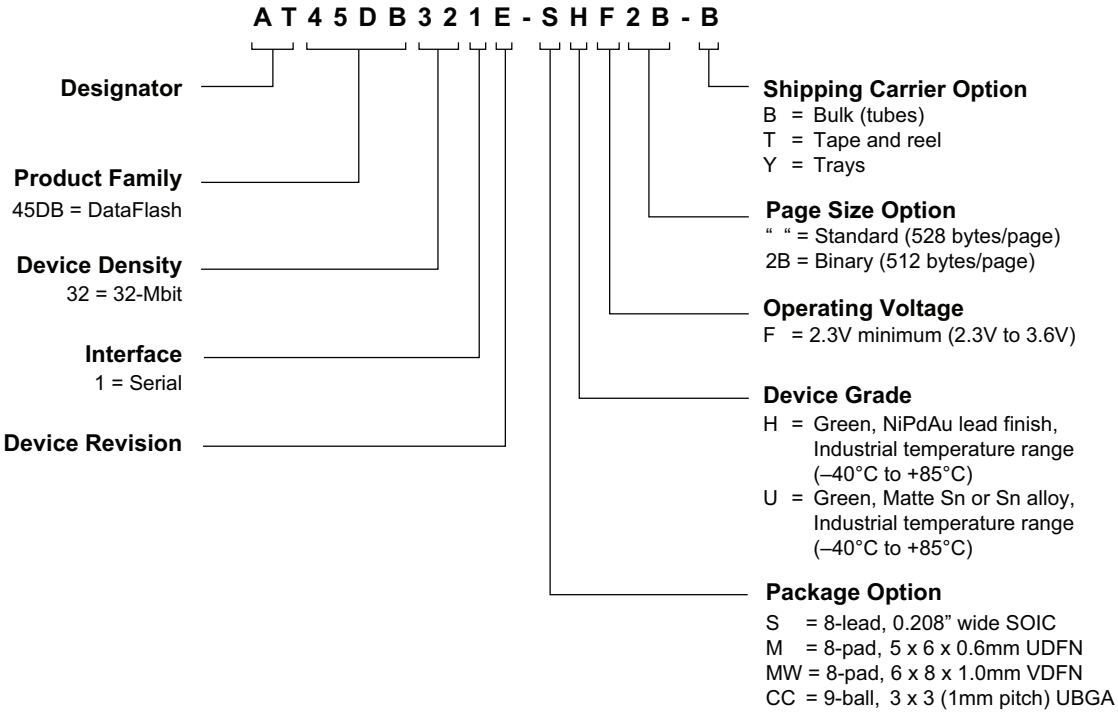
Figure 26-2. Algorithm for Programming or Re-programming of the Entire Array Randomly



Notes:
1. To preserve data integrity, each page of an DataFlash sector must be updated/rewritten at least once within every 50,000 cumulative page erase and program operations
2. A page address pointer must be maintained to indicate which page is to be rewritten. The auto page rewrite command must use the address specified by the page address pointer
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications may choose to wait until 50,000 cumulative page erase and program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Adesto’s Serial DataFlash”) for more details

27. Ordering Information

27.1 Ordering Detail



27.2 Ordering Codes (Standard DataFlash Page Size)

Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB321E-SHF-B(1)	8S2	NiPdAu	2.3V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB321E-SHF-T(1)					
AT45DB321E-MWHF-Y(1)	8MW1				
AT45DB321E-MWHF-T(1)					
AT45DB321E-CCUF-T(1)	9CC1	SnAgCu			
AT45DB321E-MHF-Y(1)	8MA1	NiPdAu	2.3V to 3.6V	70MHz	Industrial (-40°C to 85°C)
AT45DB321E-MHF-T(1)					

Notes: 1. The shipping carrier suffix is not marked on the device.

27.3 Ordering Codes (Binary Page Size)

Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB321E-SHF2B-T(1)(2)	8S2	NiPdAu	2.3V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB321E-MWHF2B-T (1)(2)	8MW1				
AT45DB321E-MHF2B-T(1)(2)	8MA1	NiPdAu	2.3V to 3.6V	70MHz	Industrial (-40°C to 85°C)

Notes: 1. The shipping carrier suffix is not marked on the device.
2. Parts ordered with suffix code ‘2B’ are shipped in tape and reel (T&R) with the page size set to 512 bytes. This option is only available for shipping in T&R (-T).

Package Type	
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6mm body) Thermally Enhanced Plastic Ultra Thin Dual Flat No-lead (UDFN)
9CC1	9-ball (6 x 6 x 0.6mm body) 3 x 3 array x 1mm pitch, Ultra-thin Ball Grid Array (UBGA)
8MW1	8-contact, 6 x 8mm, Very Thin Dual Flat No Lead Package (VDFN)

27.4 Ordering Codes (Reserved)

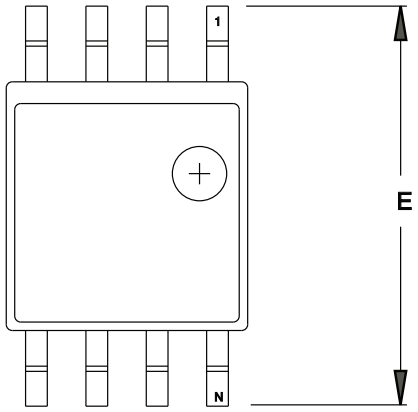
Ordering Code	Package	Lead Finish	Operating Voltage	f_{SCK}	Device Grade
AT45DB321E-SHFHA-T[1][2]	8S2	NiPdAu	2.3V to 3.6V	85MHz	Industrial (-40°C to 85°C)
AT45DB321E-SHFHC-T[1][3]					

Notes:
1. The shipping carrier suffix is not marked on the device.
2. Parts ordered with suffix code ‘HA’ are shipped in tape and reel (T&R) only with the page size set to 528 bytes.
3. Parts ordered with suffix code ‘HC’ are shipped in tape and reel (T&R) only with the page size set to 512 bytes.
4. Please contact Adesto for a description of these ‘Reserved’ codes.

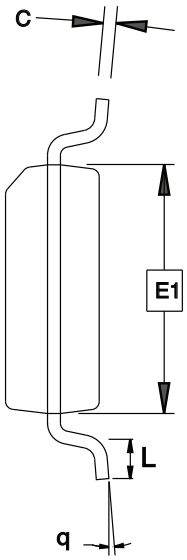
Package Type	
8S2	8-lead 0.208" wide, Plastic Gull Wing Small Outline (EIAJ SOIC)

28. Packaging Information

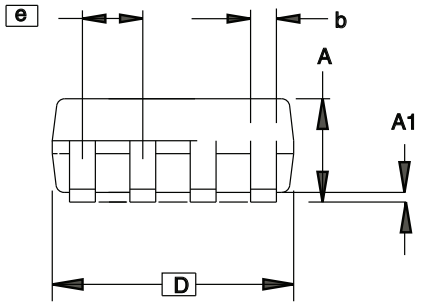
28.1 8S2 – 8-lead EIAJ SOIC



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

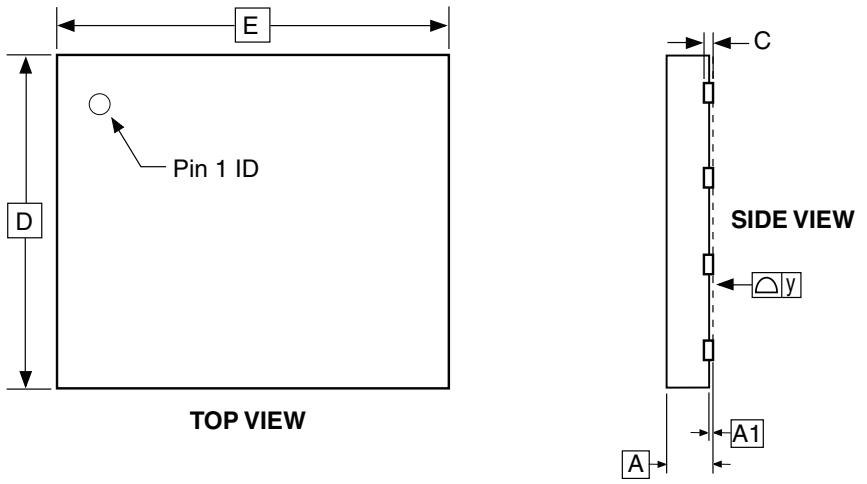
SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
q	0°		8°	
e	1.27 BSC			3

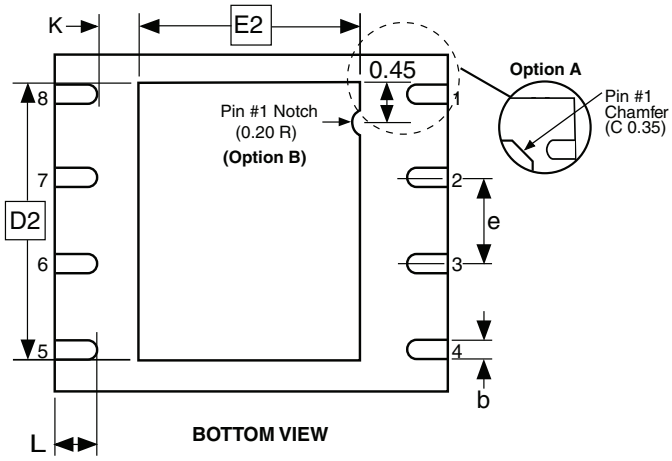
Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

4/15/08

adesto™ TECHNOLOGIES **Package Drawing Contact:** contact@adestotech.com	**TITLE** **8S2,** 8-lead, 0.208" Body, Plastic Small Outline Package (EIAJ)	**GPC** STN	**DRAWING NO.** 8S2	**REV.** F

28.2 8MA1 – 8-pad UDFN





COMMON DIMENSIONS
(Unit of Measure = mm)

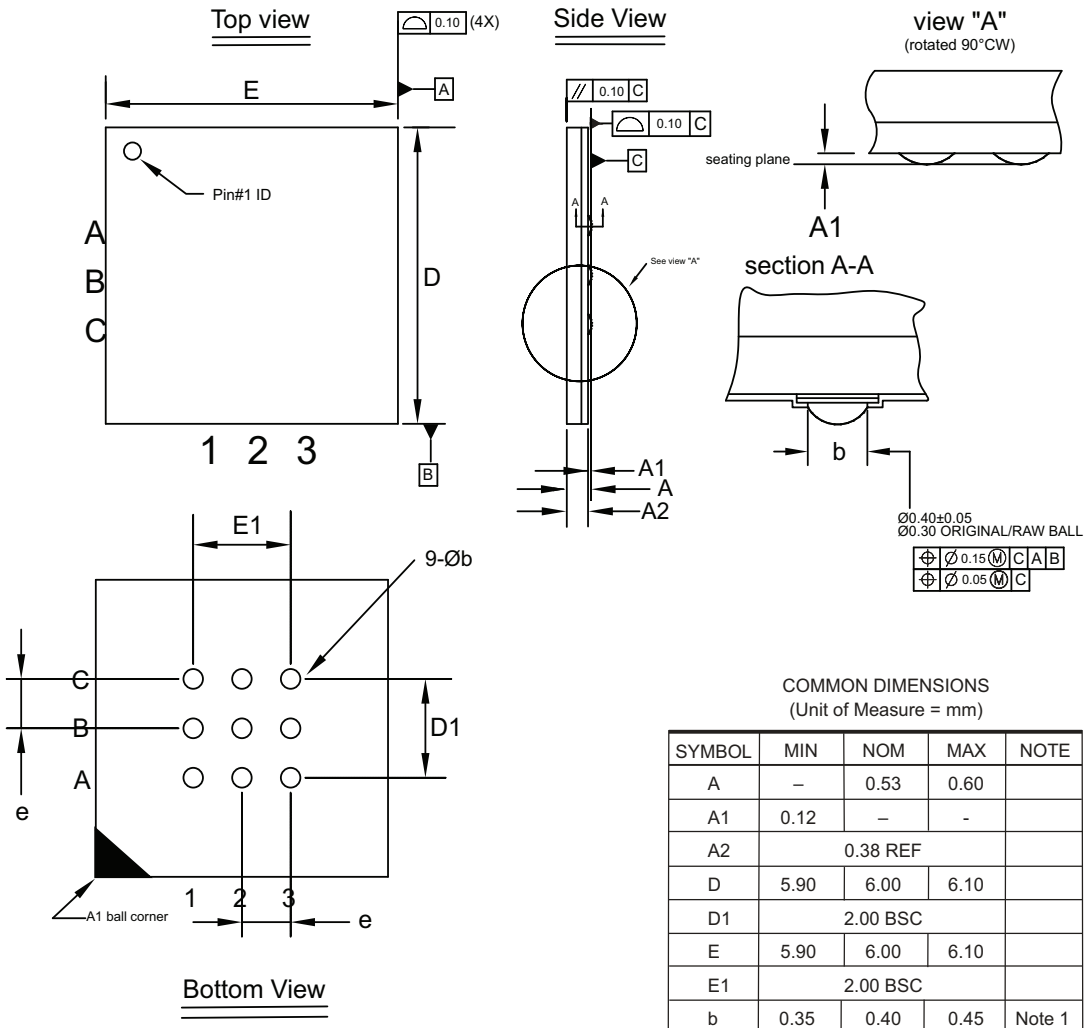
SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
adesto TECHNOLOGIES **Package Drawing Contact:** contact@adestotech.com	**8MA1,** 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YFG	8MA1	D

28.3 9CC1 — 9-ball UBGA



COMMON DIMENSIONS
(Unit of Measure = mm)

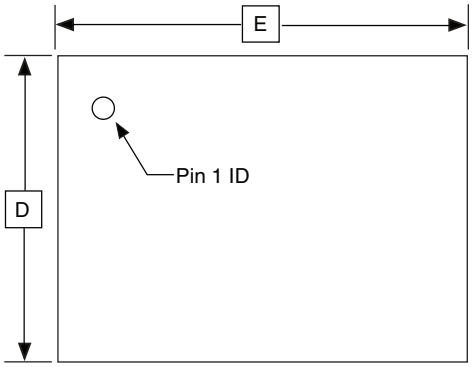
SYMBOL	MIN	NOM	MAX	NOTE
A	–	0.53	0.60	
A1	0.12	–	-	
A2		0.38 REF		
D	5.90	6.00	6.10	
D1		2.00 BSC		
E	5.90	6.00	6.10	
E1		2.00 BSC		
b	0.35	0.40	0.45	Note 1
e		1.00 BSC		

Notes: 1. Dimension “b” is measured at the maximum ball diameter, in a plane parallel to the seating plane.

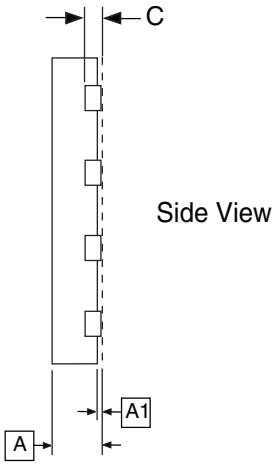
6/30/09

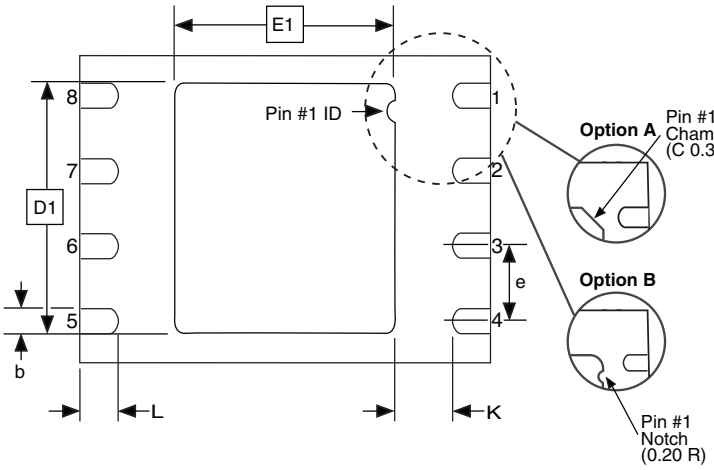
adesto TECHNOLOGIES **Package Drawing Contact:** contact@adestotech.com	**TITLE** **9CC1**, 9-ball, 6 x 6 x 0.6mm Body, 1.0mm ball pitch (3x3 Array), Ultra-thin Ball Grid Array Package(UBGA)	**GPC** CAA	**DRAWING NO.** 9CC1	**REV.** A

28.4 8 MWH – 8-pad VDFN



Top View





Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	–	1.00	
A1	–	–	0.05	
b	0.35	0.40	0.48	
C		0.203 REF		
D	5.90	6.00	6.10	
D1	4.70	4.80	4.90	
E	7.90	8.00	8.10	
E1	4.80	4.90	5.00	
e		1.27		
L	0.45	0.50	0.55	
K		1.05 REF		

1/12/09

adesto TECHNOLOGIES **Package Drawing Contact:** contact@adestotech.com	**TITLE** **8MW1**, 8-pad (6 x 8 x 1.0 mm Body), Thermally Enhanced Plastic Very Thin Dual Flat No Lead Package (VDFN)	**DRAWING NO.** 8MW1	**REV.** E

29. Revision History

Doc. Rev.	Date	Comments
8784F	11/2013	Corrected Product ID Values for Byte 2 in Figure 12.1, Table 12.1 and Table 12.2. Corrected Memory Architecture Diagram, Figure 3-1.
8784E	10/2013	Updated spec in Continuous Array Read (1Bh Opcode) to f_{CAR4}. Corrected Low Power Read Option (up to 15MHz). Corrected Ultra-Deep Power-Down current (400nA typical). Updated spec for Input High Voltage (Max) to V_{CC} + 0.6V.
8784D	7/2013	Updated Auto Page Rewrite cycle to 50,000 cumulative page erase/program operations. Corrected Page Erase and Programming Time specification to 35 ms maximum. Updated DC conditions for V_{OL}, I_{CC3} and I_{CC4}. Added reserved part order codes. Changed datasheet status from preliminary to complete.
8784C	6/2013	Updated electrical and power specifications. “Buffer 1 (or 2) Read” moved from group C to Group A in Operation Mode Summary. Removed references to 2.5V minimum power supply.
8784B	11/2012	Added Legacy Commands table. Updated to Adesto template.
8784A	08/2012	Initial document release.

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