C8051F340/1/2/3/4/5/6/7/8/9

Full Speed USB Flash MCU Family

Analog Peripherals
- **10-Bit ADC ('F340/1/2/3/4/5/6/7 only)**
  - Up to 200 ksps
  - Built-in analog multiplexer with single-ended and differential mode
  - VREF from external pin, internal reference, or V_{DD}
  - Built-in temperature sensor
  - External conversion start input option
- **Two comparators**
- **Internal voltage reference ('F340/1/2/3/4/5/6/7 only)**
- **Brown-out detector and POR Circuitry**

USB Function Controller
- USB specification 2.0 compliant
- Full speed (12 Mbps) or low speed (1.5 Mbps) operation
- Integrated clock recovery; no external crystal required for full speed or low speed
- Supports eight flexible endpoints
- 1 kB USB buffer memory
- Integrated transceiver; no external resistors required

On-Chip Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets

Voltage Supply Input: 2.7 to 5.25 V
- Voltages from 3.6 to 5.25 V supported using On-Chip Voltage Regulator

HIgh Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of Instructions in 1 or 2 system clocks
- 48 MIPS and 25 MIPS versions available.
- Expanded interrupt handler

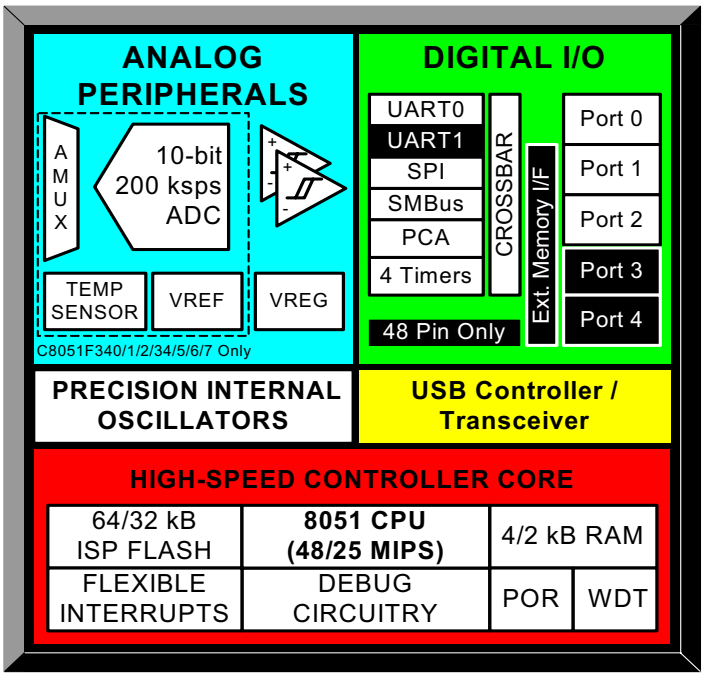
Memory
- 4352 or 2304 Bytes RAM
- 64 or 32 kB Flash; In-system programmable in 512-byte sectors

Digital Peripherals
- 40/25 Port I/O; All 5 V tolerant with high sink current
- Hardware enhanced SPI™, SMBus™, and one or two enhanced UART serial ports
- Four general purpose 16-bit counter/timers
- 16-bit programmable counter array (PCA) with five capture/compare modules
- External Memory Interface (EMIF)

Clock Sources
- Internal Oscillator: ±0.25% accuracy with clock recovery enabled. Supports all USB and UART modes
- External Oscillator: Crystal, RC, C, or clock (1 or 2 Pin modes)
- Low Frequency (80 kHz) Internal Oscillator
- Can switch between clock sources on-the-fly

Packages
- 48-pin TQFP (C8051F340/1/4/5/8)
- 32-pin LQFP (C8051F342/3/6/7/9)

Temperature Range: –40 to +85 °C



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1. System Overview

C8051F340/1/2/3/4/5/6/7/8/9 devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 48 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- Universal Serial Bus (USB) Function Controller with eight flexible endpoint pipes, integrated transceiver, and 1 kB FIFO RAM
- Supply Voltage Regulator
- True 10-bit 200 ksps differential / single-ended ADC with analog multiplexer
- On-chip Voltage Reference and Temperature Sensor
- On-chip Voltage Comparators (2)
- Precision internal calibrated 12 MHz internal oscillator and 4x clock multiplier
- Internal low-frequency oscillator for additional power savings
- Up to 64 kB of on-chip Flash memory
- Up to 4352 Bytes of on-chip RAM (256 + 4 kB)
- External Memory Interface (EMIF) available on 48-pin versions.
- SMBus/I2C, up to 2 UARTs, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Missing Clock Detector
- Up to 40 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Voltage Regulator, Watchdog Timer, and clock oscillator, C8051F340/1/2/3/4/5/6/7/8/9 devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system debugging without occupying package pins.

Each device is specified for 2.7–5.25 V operation over the industrial temperature range (–40 to +85 °C). For voltages above 3.6 V, the on-chip Voltage Regulator must be used. A minimum of 3.0 V is required for USB communication. The Port I/O and /RST pins are tolerant of input signals up to 5 V. C8051F340/1/2/3/4/5/6/7/8/9 devices are available in 48-pin TQFP or 32-pin LQFP packages. See Table 1.1, “Product Selection Guide,” on page 22 for feature and package choices.

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (Bytes)	RAM	Calibrated Internal Oscillator	Low Frequency Oscillator	USB with 1k Endpoint RAM	Supply Voltage Regulator	SMBus/I2C	Enhanced SPI	UARTs	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	External Memory Interface (EMIF)	10-bit 200ksps ADC	Temperature Sensor	Voltage Reference	Analog Comparators	Package
C8051F340-GQ	48	64k	4352	✓	✓	✓	✓	✓	✓	2	4	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F341-GQ	48	32k	2304	✓	✓	✓	✓	✓	✓	2	4	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F342-GQ	48	64k	4352	✓	✓	✓	✓	✓	✓	1	4	✓	25	—	✓	✓	✓	2	LQFP32
C8051F343-GQ	48	32k	2304	✓	✓	✓	✓	✓	✓	1	4	✓	25	—	✓	✓	✓	2	LQFP32
C8051F344-GQ	25	64k	4352	✓	✓	✓	✓	✓	✓	2	4	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F345-GQ	25	32k	2304	✓	✓	✓	✓	✓	✓	2	4	✓	40	✓	✓	✓	✓	2	TQFP48
C8051F346-GQ	25	64k	4352	✓	—	✓	✓	✓	✓	1	4	✓	25	—	✓	✓	✓	2	LQFP32
C8051F347-GQ	25	32k	2304	✓	—	✓	✓	✓	✓	1	4	✓	25	—	✓	✓	✓	2	LQFP32
C8051F348-GQ	25	32k	2304	✓	✓	✓	✓	✓	✓	2	4	✓	40	✓	—	—	—	2	TQFP48
C8051F349-GQ	25	32k	2304	✓	✓	✓	✓	✓	✓	1	4	✓	25	—	—	—	—	2	LQFP32

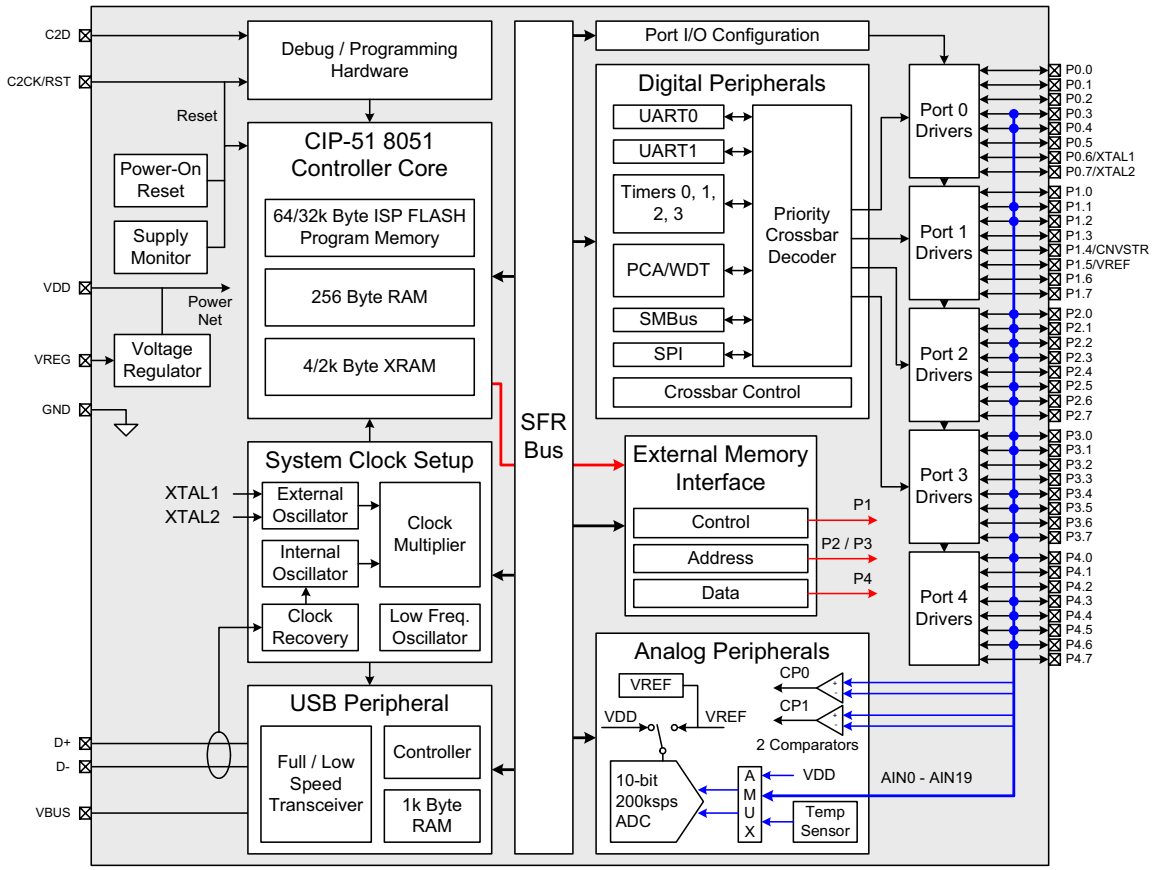

Figure 1.1. C8051F340/1/4/5 Block Diagram

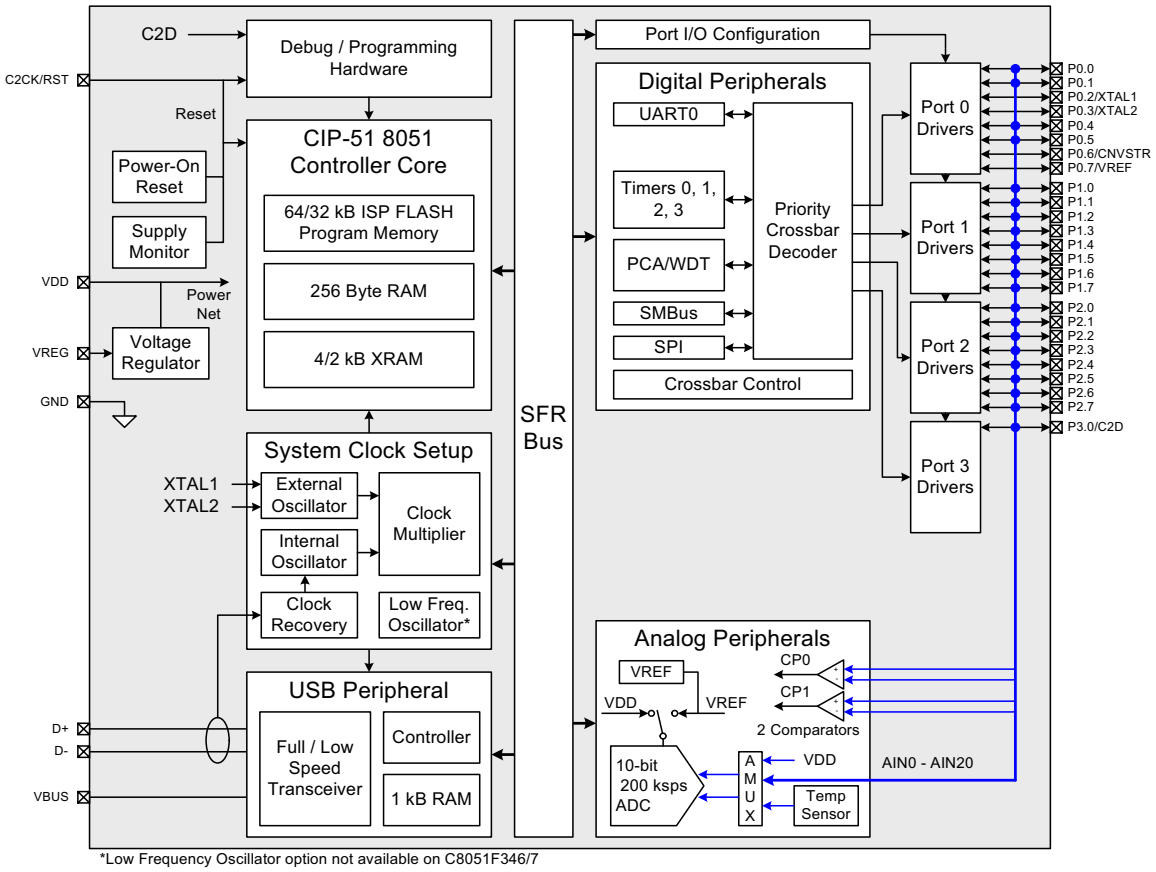

Figure 1.2. C8051F342/3/6/7 Block Diagram

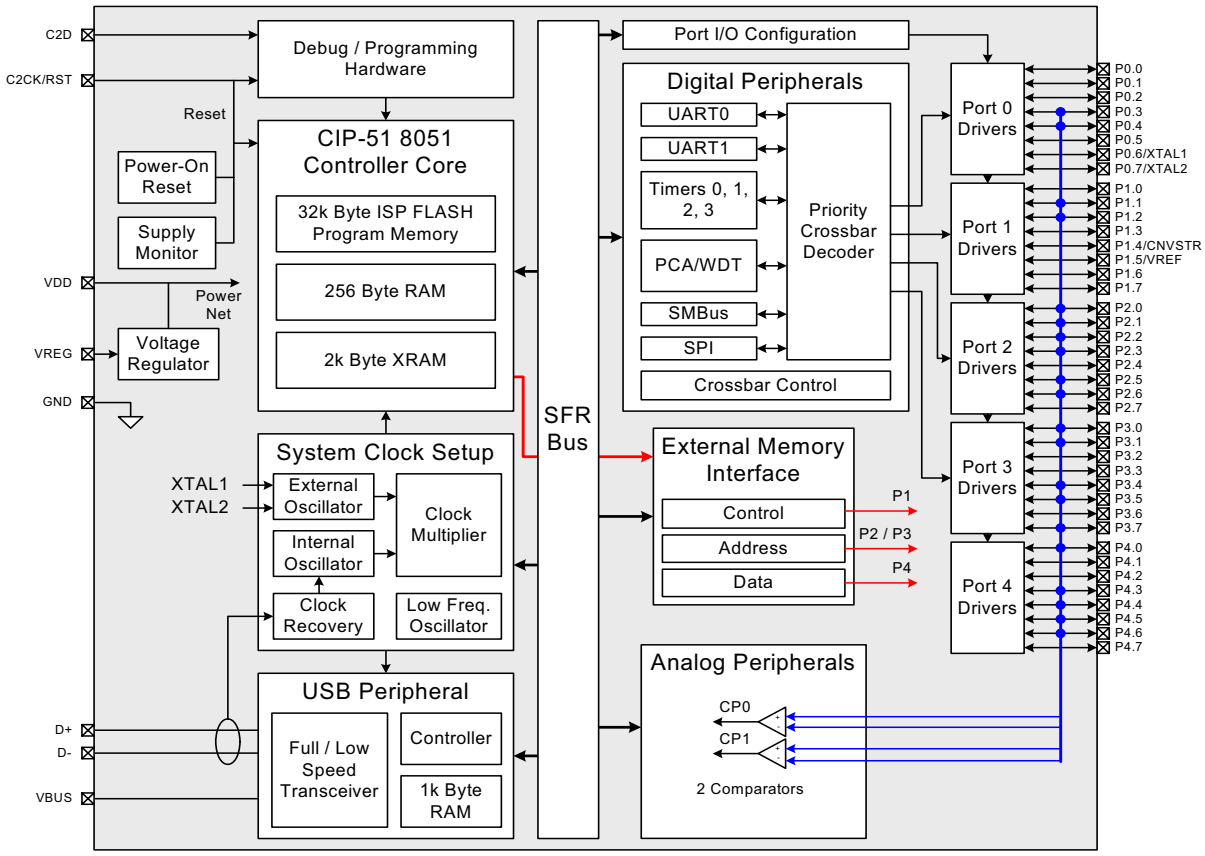

Figure 1.3. C8051F348 Block Diagram

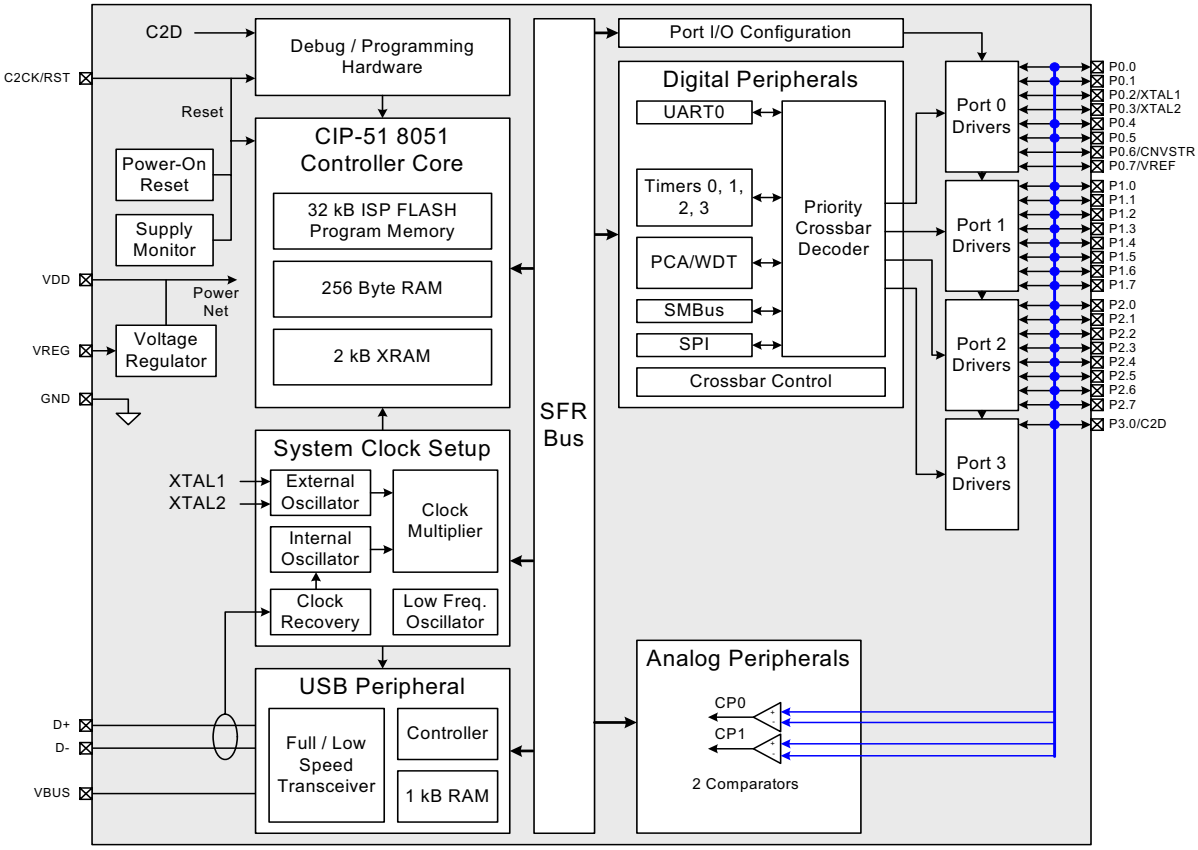

Figure 1.4. C8051F349 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F340/1/2/3/4/5/6/7/8/9 family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including four 16-bit counter/timers, two full-duplex UARTs with extended baud rate configuration, an enhanced SPI port, up to 4352 Bytes of on-chip RAM, 128 byte Special Function Register (SFR) address space, and up to 40 I/O pins.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions listed by the required execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

1.1.3. Additional Features

The C8051F340/1/2/3/4/5/6/7/8/9 SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 16 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Nine reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below V_{RST} as given in Table 11.1 on page 117), the USB controller (USB bus reset or a VBUS transition), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an errant Flash read/write protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The high-speed internal oscillator is factory calibrated to 12 MHz ±1.5%. A clock recovery mechanism allows the internal oscillator to be used with the 4x Clock Multiplier as the USB clock source in Full Speed mode; the internal oscillator can also be used as the USB clock source in Low Speed mode. External oscillators may also be used with the 4x Clock Multiplier. An internal low-frequency oscillator is also included to aid applications where power savings are critical. Also included is an external oscillator drive circuit, which allows an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. The system clock may be configured to use ether of the internal oscillators, an external oscillator, or the Clock Multiplier output divided by 2. If desired, the system clock source may be switched on-the-fly between oscillator sources. The low-frequency internal oscillator or an external oscillator can be useful in low power applications, allowing the MCU to run from a slow (power saving) external clock source, while periodically switching to a higher-speed clock source when fast throughput is necessary.

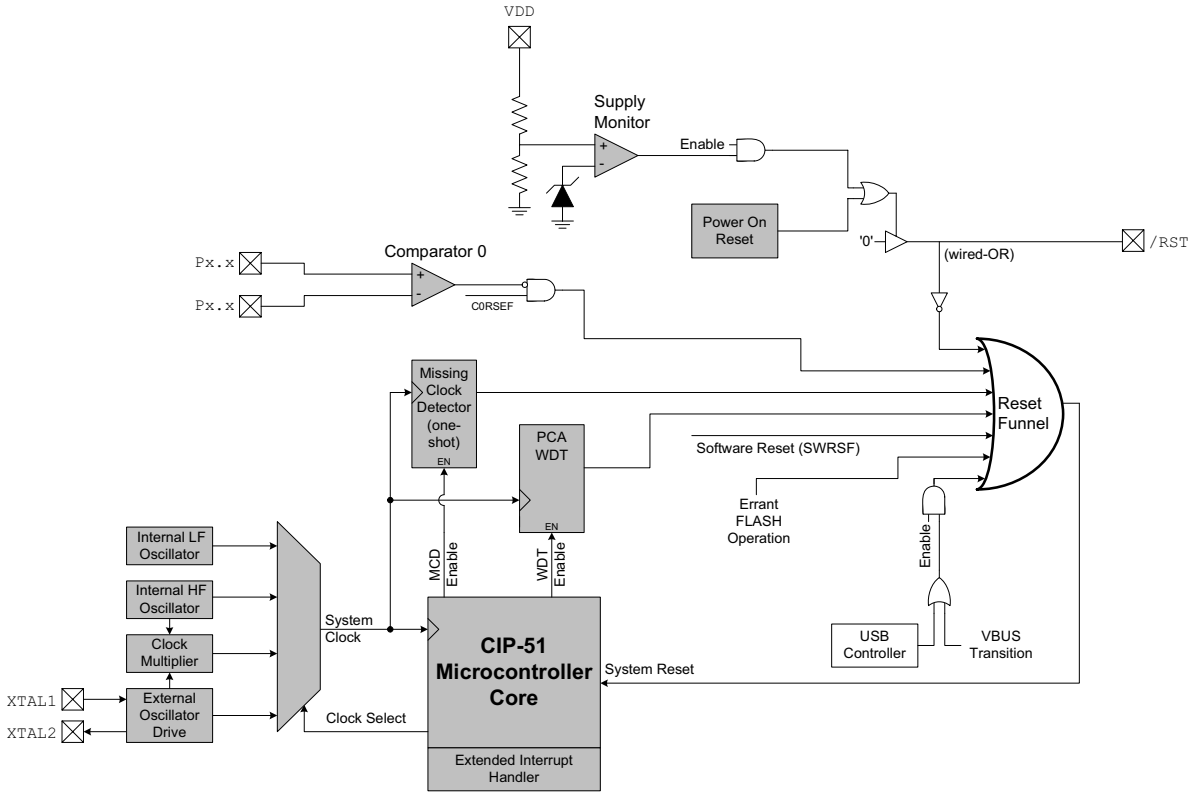

Figure 1.5. On-Chip Clock and Reset

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 64 k (C8051F340/2/4/6) or 32 k (C8051F341/3/5/7/8/9) bytes of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. On-chip XRAM is also included for the entire device family. The 64 k FLASH devices (C8051F340/2/4/6) have 4 k of XRAM space. The 32 k Flash devices (C8051F341/3/5/7/8/9) have 2 k of XRAM space. A separate 1 k Bytes of USB FIFO RAM is also included on all devices. See Figure 1.6 for the MCU system memory map of the 64k Flash devices. Note that on the 64k devices, 1024 bytes at locations 0xFC00 to 0xFFFF are reserved. See Figure 1.8 for the MCU system memory map of the 32k Flash devices.

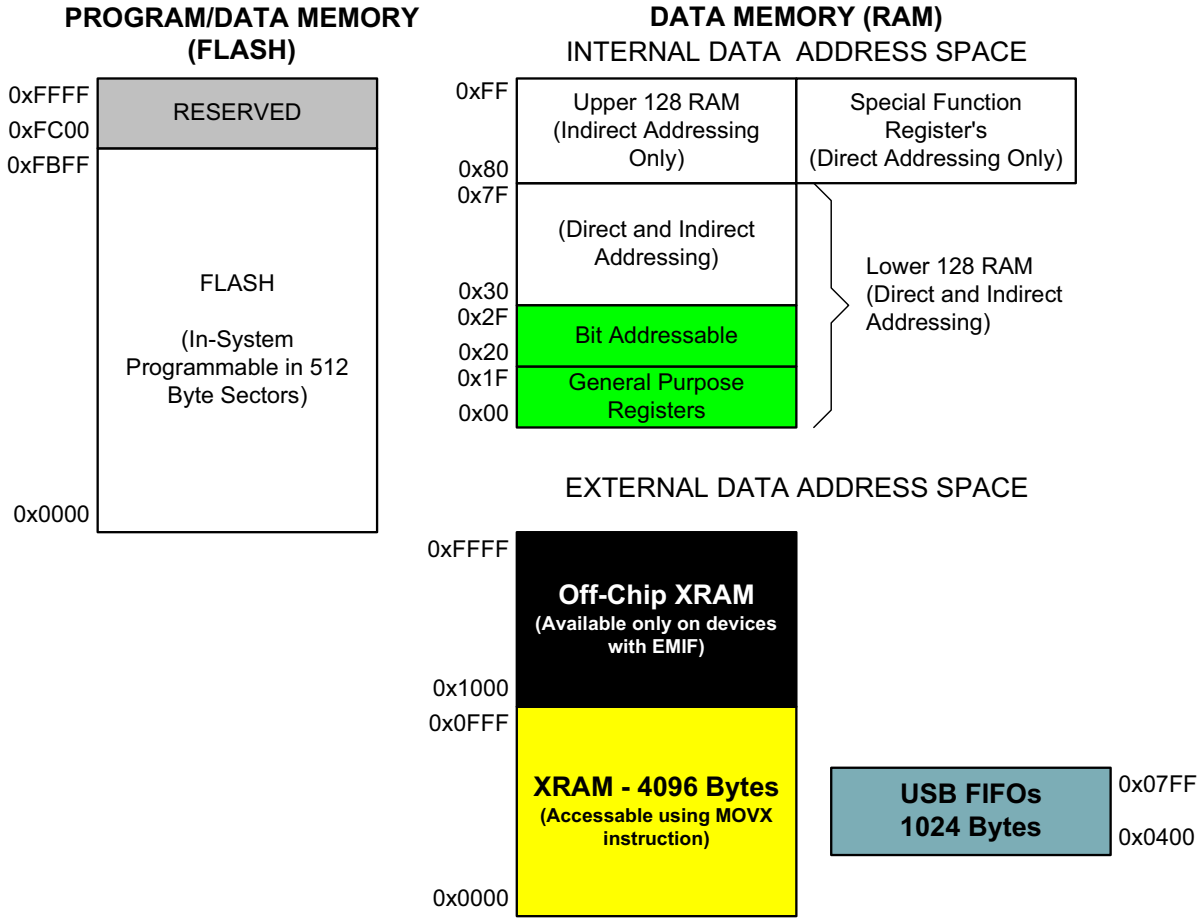

Figure 1.6. On-Chip Memory Map for 64kB Devices (C8051F340/2/4/6)

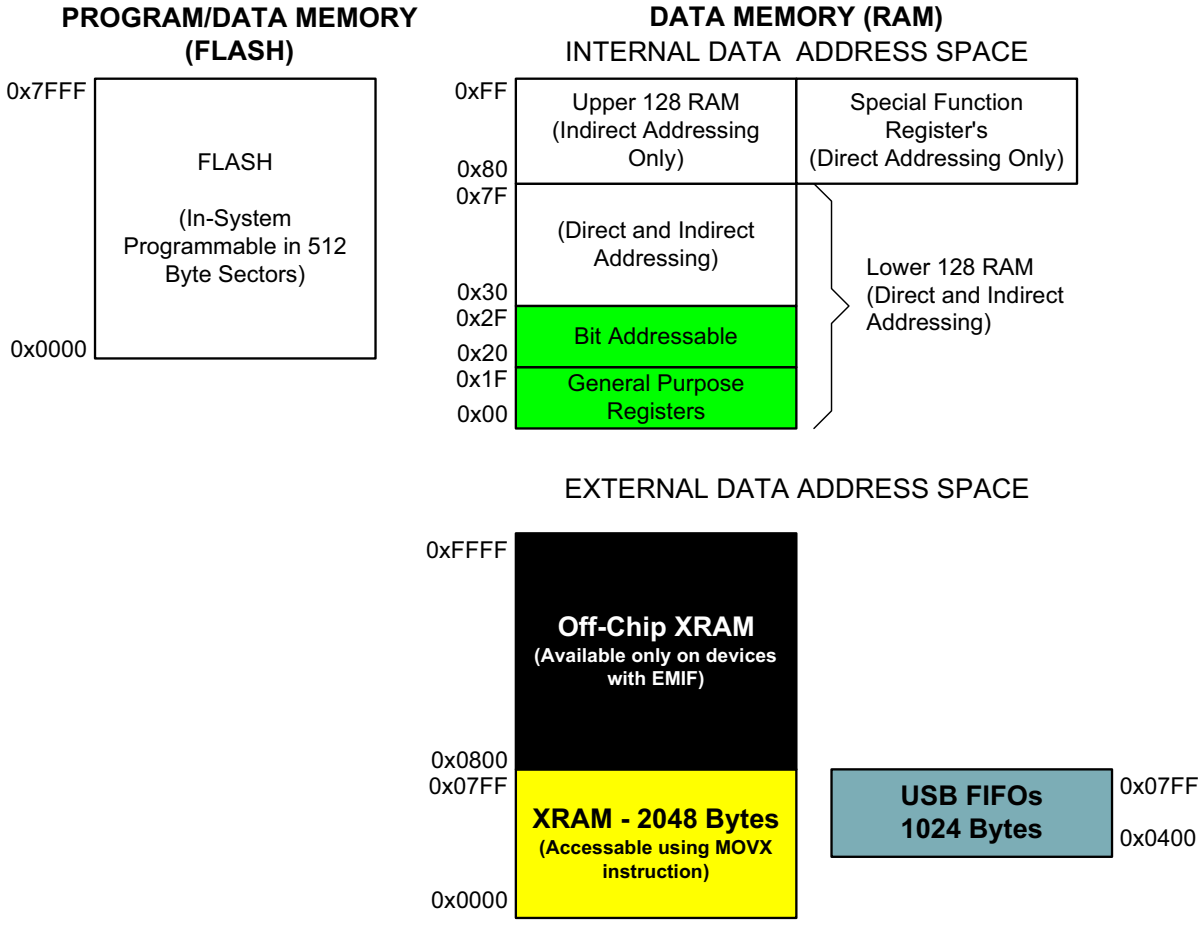

Figure 1.7. On-Chip Memory Map for 32 kB Devices (C8051F341/3/5/7/8/9)

1.3. Universal Serial Bus Controller

The Universal Serial Bus Controller (USB0) is a USB 2.0 compliant Full or Low Speed function with integrated transceiver and endpoint FIFO RAM. A total of eight endpoint pipes are available: a bi-directional control endpoint (Endpoint0) and three pairs of IN/OUT endpoints (Endpoints1-3 IN/OUT).

A 1k Byte block of RAM is used for USB FIFO space. This FIFO space is distributed among Endpoints0-3; Endpoint1-3 FIFO slots can be configured as IN, OUT, or both IN and OUT (split mode). The maximum FIFO size is 512 bytes (Endpoint3).

USB0 can be operated as a Full or Low Speed function. On-chip 4x Clock Multiplier and clock recovery circuitry allow both Full and Low Speed options to be implemented with the on-chip precision oscillator as the USB clock source. An external oscillator source can also be used with the 4x Clock Multiplier to generate the USB clock. The CPU clock source is independent of the USB clock.

The USB Transceiver is USB 2.0 compliant, and includes on-chip matching and pull-up resistors. The pull-up resistors can be enabled/disabled in software, and will appear on the D+ or D- pin according to the software-selected speed setting (Full or Low Speed).

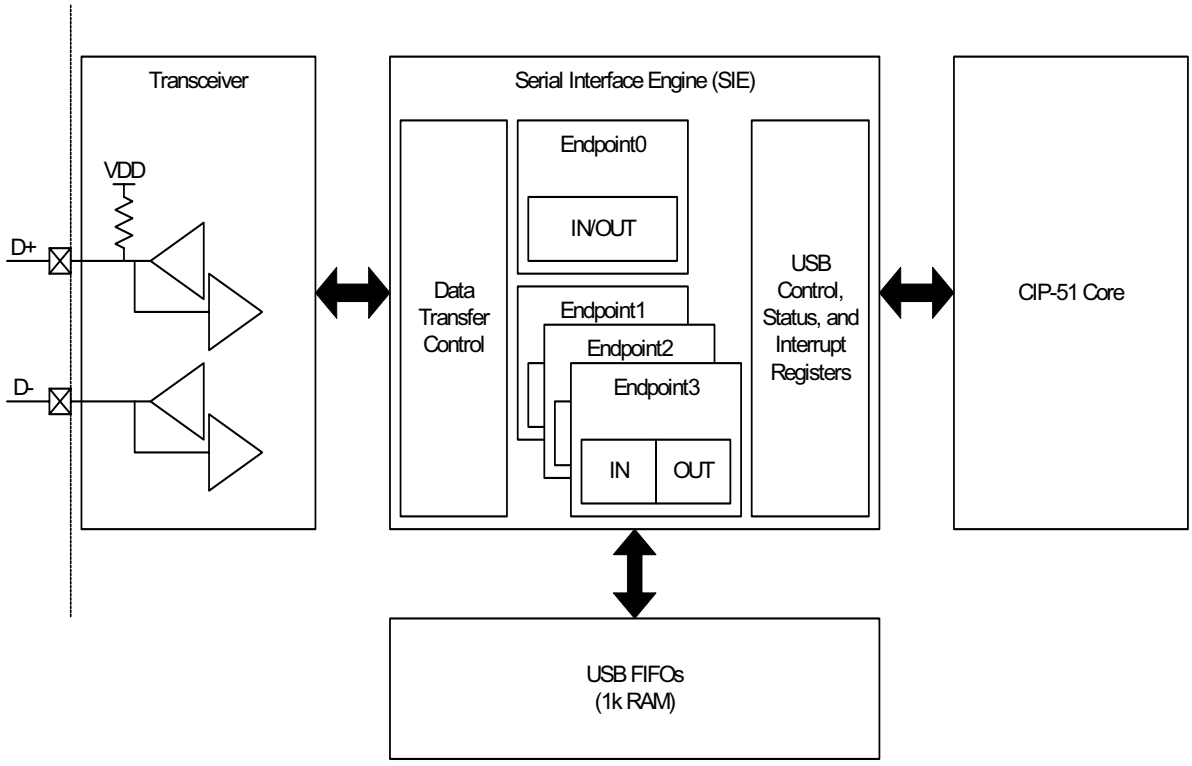

Figure 1.8. USB Block Diagram

1.4. Voltage Regulator

C8051F340/1/2/3/4/5/6/7/8/9 devices include a voltage regulator (REG0). When enabled, the REG0 output appears on the V_{DD} pin, and can also be used to power other external devices. REG0 can be enabled/disabled by software.

1.5. On-Chip Debug Circuitry

The C8051F340/1/2/3/4/5/6/7/8/9 devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the USB, ADC, and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F340DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F340/1/2/3/4/5/6/7/8/9 MCUs. The kit includes software with a developer's studio and debugger, 8051 assembler and linker, evaluation ‘C’ compiler, and a debug adapter. It also has a target application board with the C8051F340 MCU installed, the necessary cables for connection to a PC, and a wall-mount power supply. The development kit contents may also be used to program and debug the device on the production PCB using the appropriate connections for the programming pins.

The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

1.6. Programmable Digital I/O and Crossbar

C8051F340/1/4/5/8 devices include 40 I/O pins (five byte-wide Ports); C8051F342/3/6/7/9 devices include 25 I/O pins (three byte-wide Ports, and a 1-bit-wide Port). The C8051F340/1/2/3/4/5/6/7/8/9 Ports behave like typical 8051 Ports with a few enhancements. Each Port pin may be configured as an analog input or a digital I/O pin. Pins selected as digital I/Os may additionally be configured for push-pull or open-drain output. The “weak pull-ups” that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.

The Digital Crossbar allows mapping of internal digital system resources to Port I/O pins (See Figure 1.9). On-chip counter/timers, serial buses, HW interrupts, comparator outputs, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the end application.

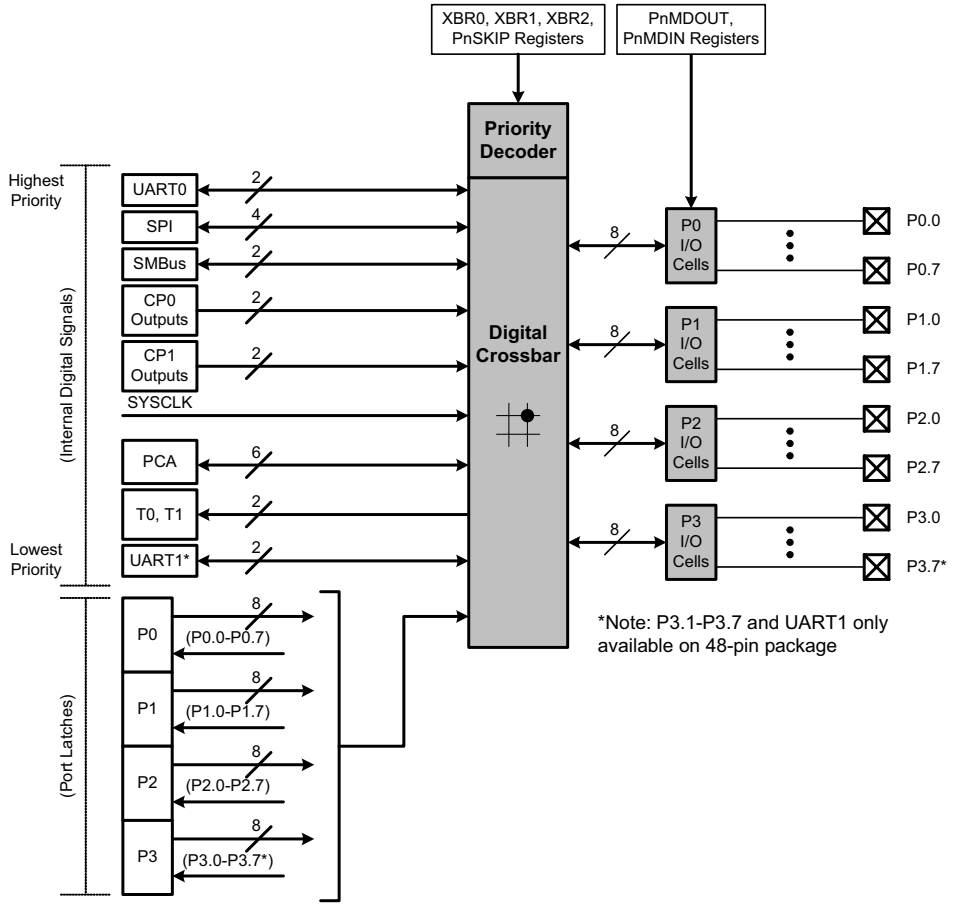

Figure 1.9. Digital Crossbar Diagram

1.7. Serial Ports

The C8051F340/1/2/3/4/5/6/7/8/9 Family includes an SMBus/I2C interface, full-duplex UARTs, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.8. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with five programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, a dedicated External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8. The external clock source selection is useful for real-time clock functionality, where the PCA may be clocked by an external source while the internal oscillator drives the system clock.

Each capture/compare module can be configured to operate in one of six modes: Edge-Triggered Capture, Software Timer, High Speed Output, 8- or 16-bit Pulse Width Modulator, or Frequency Output. Additionally, Capture/Compare Module 4 offers watchdog timer (WDT) capabilities. Following a system reset, Module 4 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

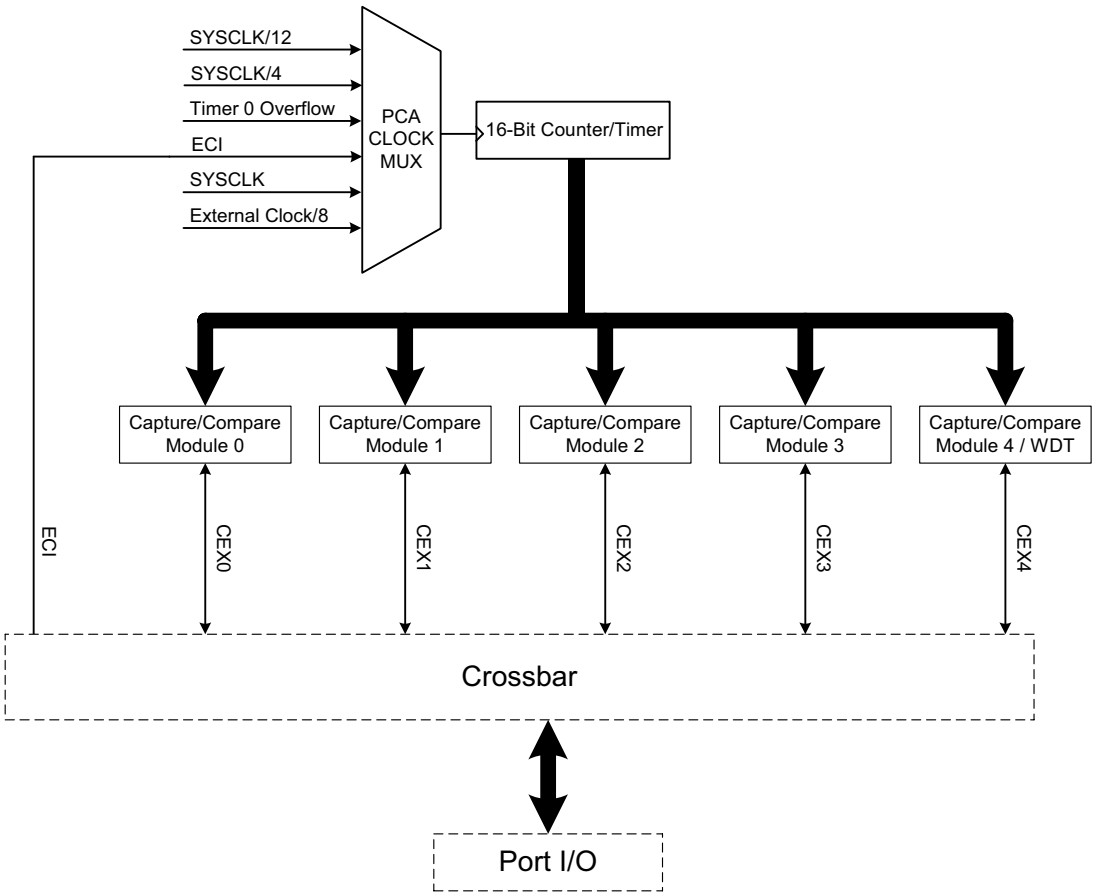

Figure 1.11. PCA Block Diagram

1.9. 10-Bit Analog to Digital Converter

The C8051F340/1/2/3/4/5/6/7 devices include an on-chip 10-bit SAR ADC with a true differential input multiplexer. With a maximum throughput of 200 ksps, the ADC offers true 10-bit linearity with an INL of ±1LSB. The ADC system includes a configurable analog multiplexer that selects both positive and negative ADC inputs. Twenty (48-pin package) or twenty-one (32-pin package) of the Port I/O pins can be used as analog inputs to the ADC. Additionally, the on-chip Temperature Sensor output and the power supply voltage (V_{DD}) are available as ADC inputs. User firmware may shut down the ADC to save power.

Conversions can be started in six ways: a software command, an overflow of Timer 0, 1, 2, or 3, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled). The resulting 10-bit data word is latched into the ADC data SFRs upon completion of a conversion.

Window compare registers for the ADC output data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

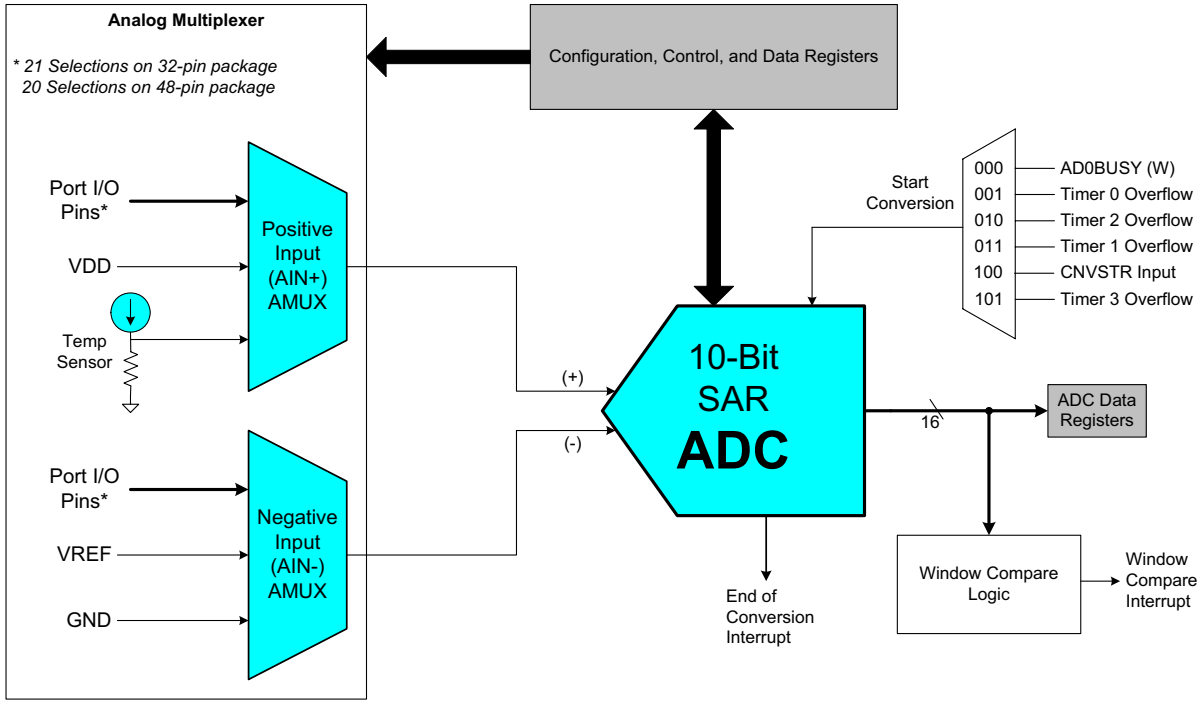

Figure 1.12. 10-Bit ADC Block Diagram

1.10. Comparators

C8051F340/1/2/3/4/5/6/7/8/9 devices include two on-chip voltage comparators that are enabled/disabled and configured via user software. Port I/O pins may be configured as comparator inputs via a selection mux. Two comparator outputs may be routed to a Port pin if desired: a latched output and/or an unlatched (asynchronous) output. Comparator response time is programmable, allowing the user to select between high-speed and low-power modes. Positive and negative hysteresis are also configurable.

Comparator interrupts may be generated on rising, falling, or both edges. When in IDLE mode, these interrupts may be used as a “wake-up” source. Comparator0 may also be configured as a reset source. Figure 1.13 shows the Comparator0 block diagram.

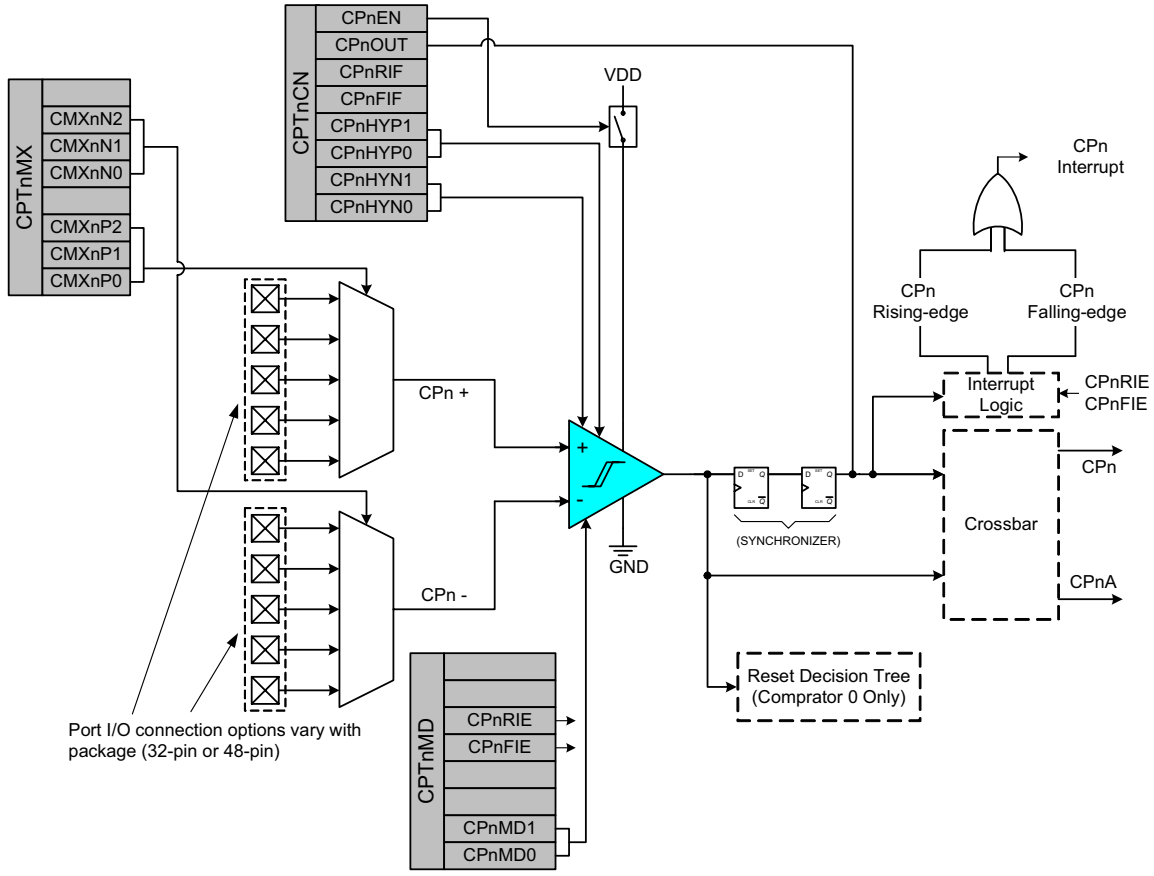

Figure 1.13. Comparator0 Block Diagram

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55		125	°C
Storage Temperature		–65		150	°C
Voltage on any Port I/O Pin or /RST with respect to GND		–0.3		5.8	V
Voltage on V_{DD} with respect to GND		–0.3		4.2	V
Maximum Total current through V_{DD} and GND				500	mA
Maximum output current sunk by /RST or any Port pin				100	mA

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. Global DC Electrical Characteristics

Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage[1]		VRST	3.3	3.6	V
Digital Supply RAM Data Retention Voltage			1.5		V
SYSCLK (System Clock)[2]	C8051F340/1/2/3 C8051F344/5/6/7/8/9	0 0		48 25	MHz
Specified Operating Temperature Range		–40		+85	°C
Digital Supply Current - CPU Active (Normal Mode, accessing Flash)					
I_{DD}[3]	V_{DD} = 3.3 V, SYSCLK = 48 MHz V_{DD} = 3.3 V, SYSCLK = 24 MHz V_{DD} = 3.3 V, SYSCLK = 1 MHz V_{DD} = 3.3 V, SYSCLK = 80 kHz V_{DD} = 3.6 V, SYSCLK = 48 MHz V_{DD} = 3.6 V, SYSCLK = 24 MHz		25.9 13.9 0.69 55 29.7 15.9	28.5 15.7 32.3 18	mA mA mA µA mA mA
I_{DD} Supply Sensitivity[3,4]	SYSCLK = 1 MHz, relative to V_{DD} = 3.3 V SYSCLK = 24 MHz, relative to V_{DD} = 3.3 V		47 46		%/V %/V
I_{DD} Frequency Sensitivity[3,5]	V_{DD} = 3.3 V, SYSCLK ≤ 30 MHz, T = 25 ºC V_{DD} = 3.3 V, SYSCLK > 30 MHz, T = 25 ºC V_{DD} = 3.6 V, SYSCLK ≤ 30 MHz, T = 25 ºC V_{DD} = 3.6 V, SYSCLK > 30 MHz, T = 25 ºC		0.69 0.44 0.80 0.50		mA/MHz mA/MHz mA/MHz mA/MHz
Digital Supply Current - CPU Inactive (Idle Mode, not accessing Flash)					
I_{DD}[3]	V_{DD} = 3.3 V, SYSCLK = 48 MHz V_{DD} = 3.3 V, SYSCLK = 24 MHz V_{DD} = 3.3 V, SYSCLK = 1 MHz V_{DD} = 3.3 V, SYSCLK = 80 kHz V_{DD} = 3.6 V, SYSCLK = 48 MHz V_{DD} = 3.6 V, SYSCLK = 24 MHz		16.6 8.25 0.44 35 18.6 9.26	18.75 9.34 20.9 10.5	mA mA mA µA mA mA
I_{DD} Supply Sensitivity[3,4]	SYSCLK = 1 MHz, relative to V_{DD} = 3.3 V SYSCLK = 24 MHz, relative to V_{DD} = 3.3 V		41 39		%/V %/V

Table 3.1. Global DC Electrical Characteristics (Continued)

–40 to +85 °C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
I_{DD} Frequency Sensitivity[3,6]	V_{DD} = 3.3 V, SYSCLK ≤ 1 MHz, T = 25 ºC		0.44		mA/MHz
	V_{DD} = 3.3 V, SYSCLK > 1 MHz, T = 25 ºC		0.32		mA/MHz
	V_{DD} = 3.6 V, SYSCLK ≤ 1 MHz, T = 25 ºC		0.49		mA/MHz
	V_{DD} = 3.6 V, SYSCLK > 1 MHz, T = 25 ºC		0.36		mA/MHz
Digital Supply Current (Stop Mode, shutdown)	Oscillator not running, V_{DD} monitor disabled		< 0.1		µA
Digital Supply Current for USB Module (USB Active Mode)	V_{DD} = 3.3 V, USB Clock = 48 MHz		8.69		mA
	V_{DD} = 3.6 V, USB Clock = 48 MHz		9.59		mA
Digital Supply Current for USB Module (USB Suspend Mode)	Oscillator not running V_{DD} monitor disabled		< 0.1		µA

Notes:

1. USB Requires 3.0 V Minimum Supply Voltage.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Based on device characterization of data; Not production tested.
4. Active and Inactive I_{DD} at voltages and frequencies other than those specified can be calculated using the I_{DD} Supply Sensitivity. For example, if the V_{DD} is 3.0 V instead of 3.3 V at 24 MHz: I_{DD} = 13.9 mA typical at 3.3 V and SYSCLK = 24 MHz. From this, I_{DD} = 13.9 mA + 0.46 x (3.0 V – 3.3 V) = 13.76 mA at 3.0 V and SYSCLK = 24 MHz.
5. I_{DD} can be estimated for frequencies ≤ 30 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} for > 30 MHz, the estimate should be the current at 24 MHz (or 48 MHz) minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.3 V; SYSCLK = 35 MHz, I_{DD} = 13.9 mA – (24 MHz – 35 MHz) x 0.44 mA/MHz = 18.74 mA.
6. Idle I_{DD} can be estimated for frequencies ≤ 1 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate Idle I_{DD} for > 1 MHz, the estimate should be the current at 24 MHz (or 48 MHz) minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.3 V; SYSCLK = 5 MHz, Idle I_{DD} = 8.25 mA – (24 MHz – 5 MHz) x 0.32 mA/MHz = 2.17 mA.

Other electrical characteristics tables are found in the data sheet section corresponding to the associated peripherals. For more information on electrical characteristics for a specific peripheral, refer to the page indicated in Table 3.2.

Table 3.2. Index to Electrical Characteristics Tables

Table Title	Page No.
ADC0 Electrical Characteristics	64
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Flash Electrical Characteristics	121
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4. Pinout and Package Definitions

Table 4.1. Pin Definitions for the C8051F340/1/2/3/4/5/6/7/8/9

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
V_{DD}	10	6	Power In Power Out	2.7–3.6 V Power Supply Voltage Input. 3.3 V Voltage Regulator Output. See **Section 8**.
GND	7	3		Ground.
/RST/ C2CK	13	9	D I/O D I/O	Device Reset. Open-drain output of internal POR or V_{DD} monitor. An external source can initiate a system reset by driving this pin low for at least 15 µs. See **Section 11**. Clock signal for the C2 Debug Interface.
C2D	14	-	D I/O	Bi-directional data signal for the C2 Debug Interface.
P3.0 / C2D	-	10	D I/O D I/O	Port 3.0. See **Section 15** for a complete description of Port 3. Bi-directional data signal for the C2 Debug Interface.
REGIN	11	7	Power In	5 V Regulator Input. This pin is the input to the on-chip voltage regulator.
VBUS	12	8	D In	VBUS Sense Input. This pin should be connected to the VBUS signal of a USB network. A 5 V signal on this pin indicates a USB network connection.
D+	8	4	D I/O	USB D+.
D-	9	5	D I/O	USB D–.
P0.0	6	2	D I/O or A In	Port 0.0. See **Section 15** for a complete description of Port 0.
P0.1	5	1	D I/O or A In	Port 0.1.
P0.2	4	32	D I/O or A In	Port 0.2.
P0.3	3	31	D I/O or A In	Port 0.3.
P0.4	2	30	D I/O or A In	Port 0.4.
P0.5	1	29	D I/O or A In	Port 0.5.
P0.6	48	28	D I/O or A In	Port 0.6.
P0.7	47	27	D I/O or A In	Port 0.7.

Table 4.1. Pin Definitions for the C8051F340/1/2/3/4/5/6/7/8/9 (Continued)

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
P1.0	46	26	D I/O or A In	Port 1.0. See **Section 15** for a complete description of Port 1.
P1.1	45	25	D I/O or A In	Port 1.1.
P1.2	44	24	D I/O or A In	Port 1.2.
P1.3	43	23	D I/O or A In	Port 1.3.
P1.4	42	22	D I/O or A In	Port 1.4.
P1.5	41	21	D I/O or A In	Port 1.5.
P1.6	40	20	D I/O or A In	Port 1.6.
P1.7	39	19	D I/O or A In	Port 1.7.
P2.0	38	18	D I/O or A In	Port 2.0. See **Section 15** for a complete description of Port 2.
P2.1	37	17	D I/O or A In	Port 2.1.
P2.2	36	16	D I/O or A In	Port 2.2.
P2.3	35	15	D I/O or A In	Port 2.3.
P2.4	34	14	D I/O or A In	Port 2.4.
P2.5	33	13	D I/O or A In	Port 2.5.
P2.6	32	12	D I/O or A In	Port 2.6.
P2.7	31	11	D I/O or A In	Port 2.7.
P3.0	30	-	D I/O or A In	Port 3.0. See **Section 15** for a complete description of Port 3.
P3.1	29	-	D I/O or A In	Port 3.1.
P3.2	28	-	D I/O or A In	Port 3.2.

Table 4.1. Pin Definitions for the C8051F340/1/2/3/4/5/6/7/8/9 (Continued)

Name	Pin Numbers		Type	Description
	48-pin	32-pin		
P3.3	27	-	D I/O or A In	Port 3.3.
P3.4	26	-	D I/O or A In	Port 3.4.
P3.5	25	-	D I/O or A In	Port 3.5.
P3.6	24	-	D I/O or A In	Port 3.6.
P3.7	23	-	D I/O or A In	Port 3.7.
P4.0	22	-	D I/O or A In	Port 4.0. See **Section 15** for a complete description of Port 4.
P4.1	21	-	D I/O or A In	Port 4.1.
P4.2	20	-	D I/O or A In	Port 4.2.
P4.3	19	-	D I/O or A In	Port 4.3.
P4.4	18	-	D I/O or A In	Port 4.4.
P4.5	17	-	D I/O or A In	Port 4.5.
P4.6	16	-	D I/O or A In	Port 4.6.
P4.7	15	-	D I/O or A In	Port 4.7.

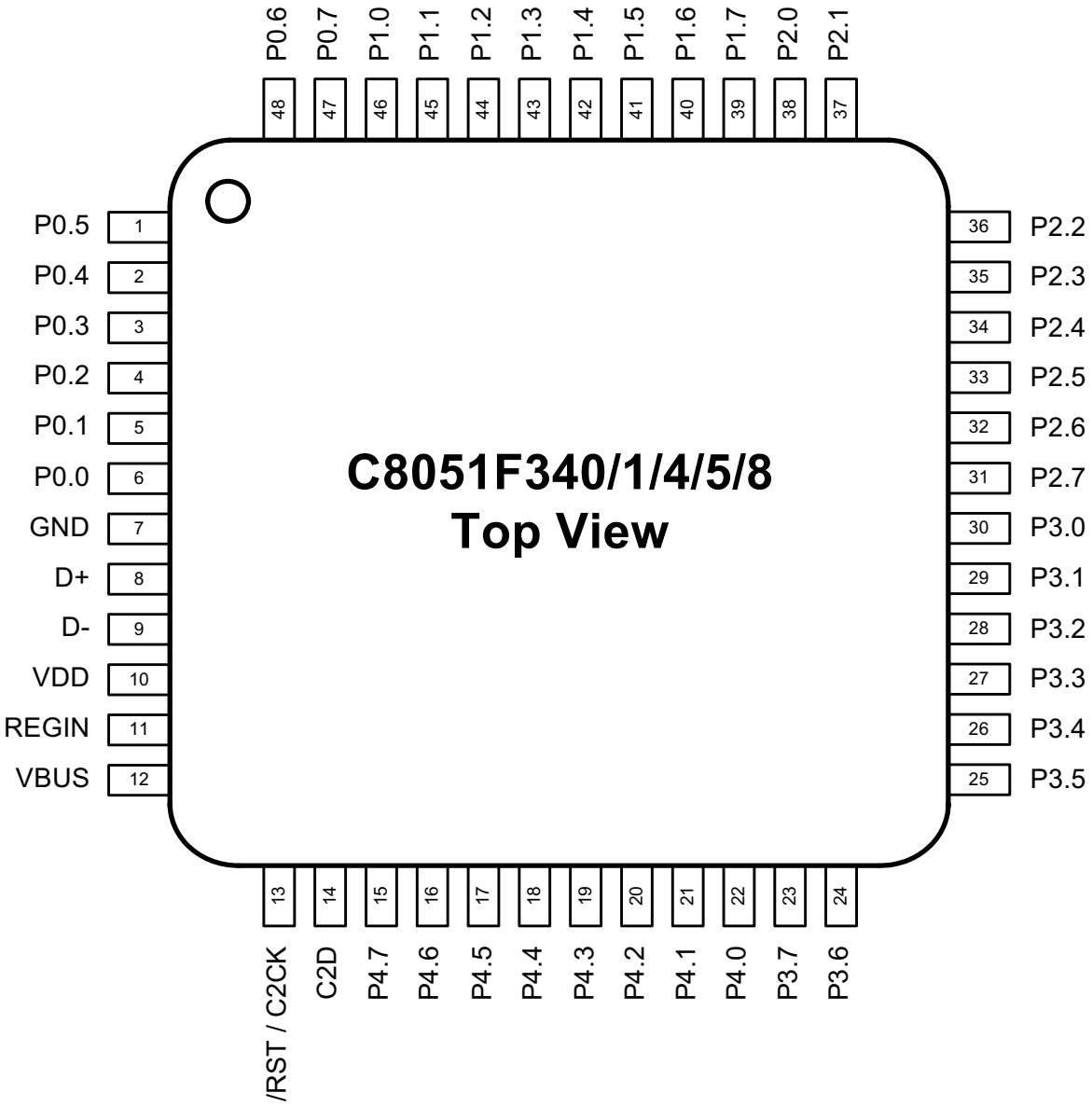

Figure 4.1. TQFP-48 Pinout Diagram (Top View)

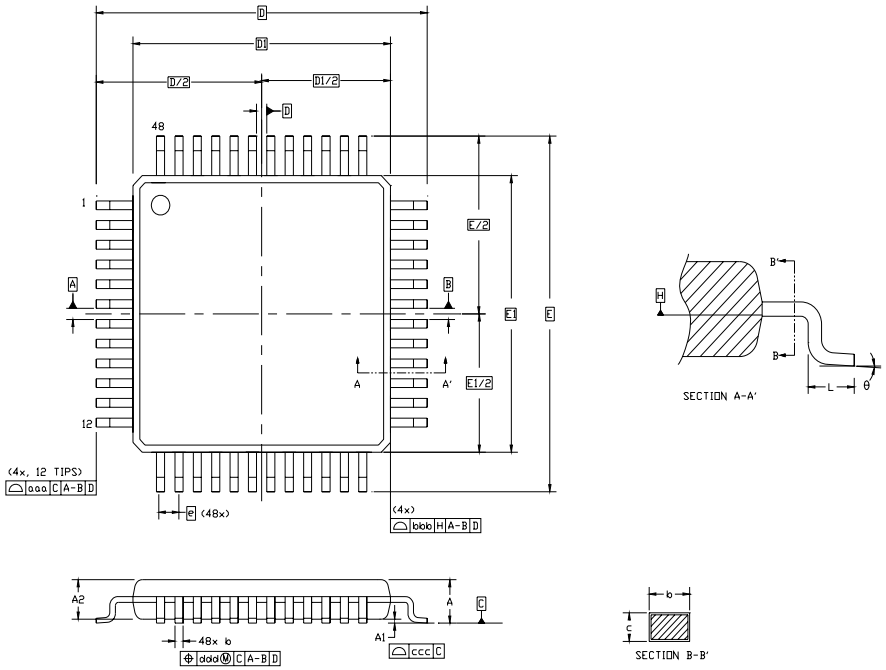

Table 4.2. TQFP-48 Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
aaa	0.20		
bbb	0.20		
ccc	0.08		
ddd	0.08		
θ	0°	3.5°	7°

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation ABC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Figure 4.2. TQFP-48 Package Diagram

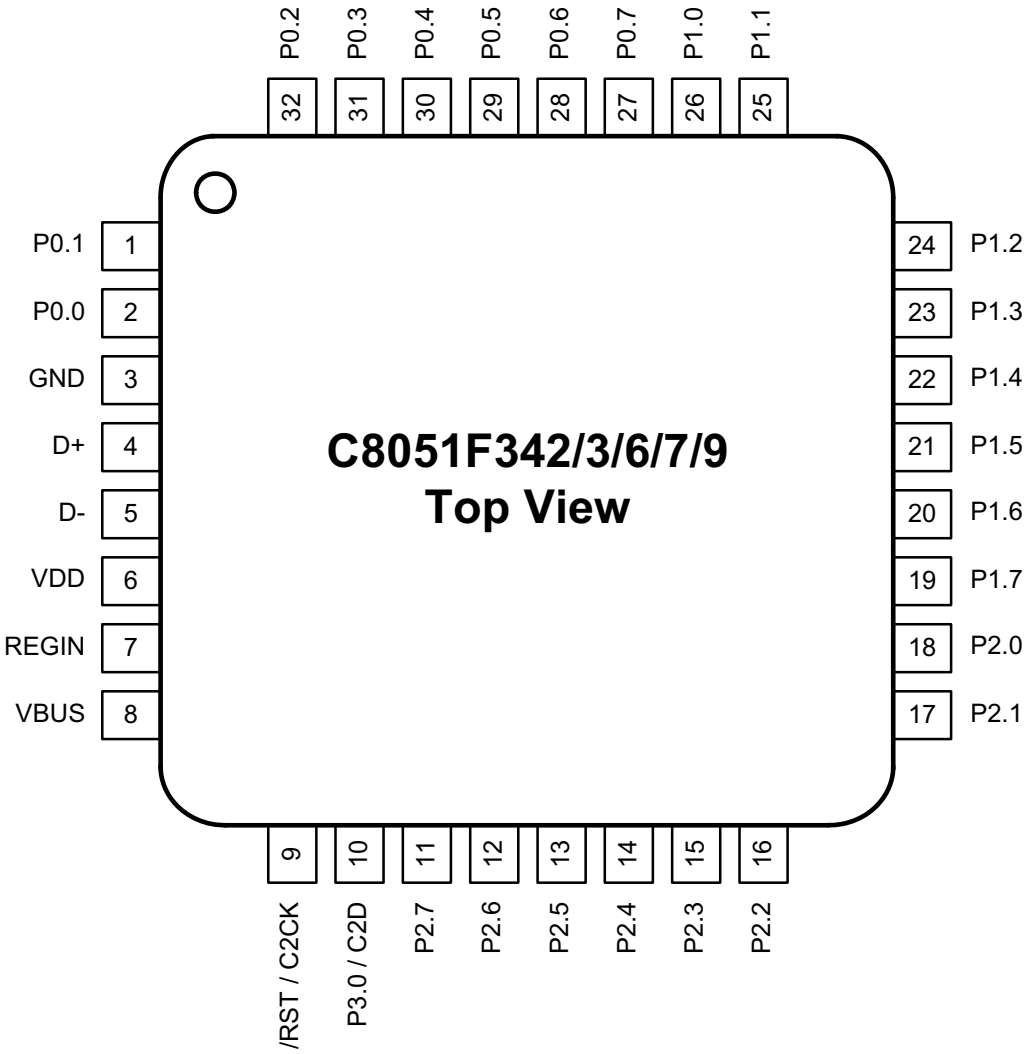

Figure 4.3. LQFP-32 Pinout Diagram (Top View)

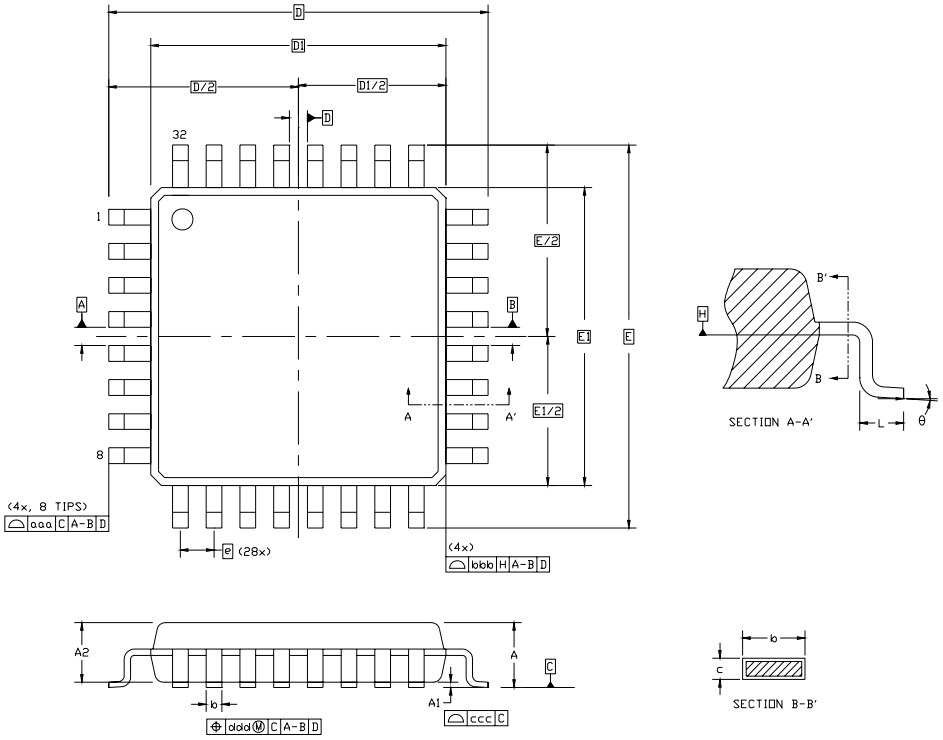

Table 4.3. LQFP-32 Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.80 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
θ	0°	3.5°	7°

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Figure 4.4. LQFP-32 Package Diagram