

## 10-Pin, 24-Bit, 192 kHz Stereo D/A Converter

### Features

- Multi-bit Delta-Sigma Modulator
- 24-Bit Conversion
- Automatically Detects Sample Rates up to 192 kHz
- 105 dB Dynamic Range
- -95 dB THD+N
- Low Clock Jitter Sensitivity
- Single +3.3 V or +5 V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis
- Popguard™ Technology
- Small 10-Pin TSSOP Package

### Description

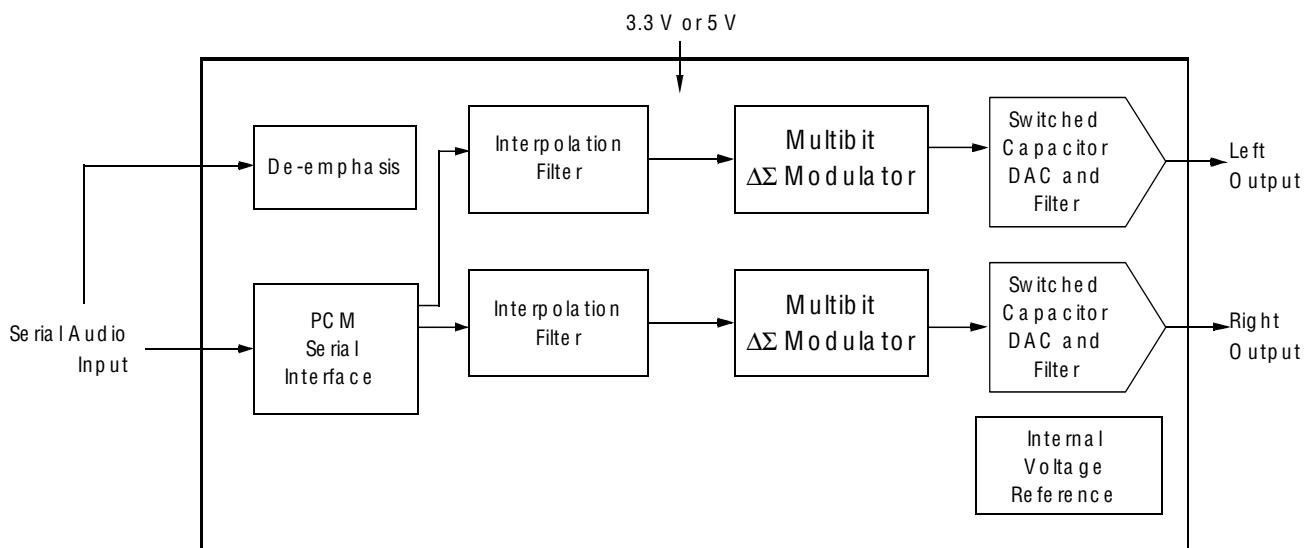
The CS4344 family members are complete, stereo digital-to-analog output systems including interpolation, multi-bit D/A conversion and output analog filtering in a 10-pin package. The CS4344/5/6/8 support all major audio data interface formats, and the individual devices differ only in the supported interface format.

The CS4344 family is based on a fourth order multi-bit delta-sigma modulator with a linear analog low-pass filter. This family also includes auto-speed mode detection using both sample rate and master clock ratio as a method of auto-selecting sampling rates between 2 kHz and 200 kHz.

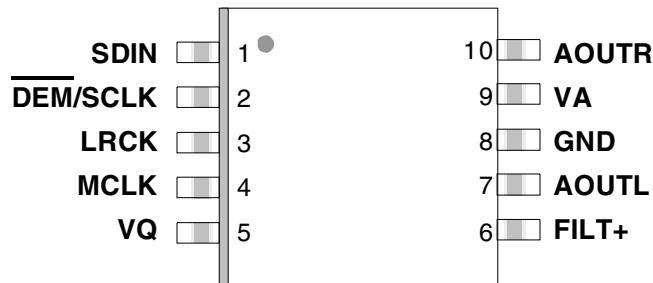
The CS4344 family contains on-chip digital de-emphasis, operates from a single +3.3 V or +5 V power supply, and requires minimal support circuitry. These features are ideal for DVD players & recorders, digital televisions, home theater and set top box products, and automotive audio systems.

### ORDERING INFORMATION

See page 19



## 1.PIN DESCRIPTIONS



Pin Name	#	Pin Description
<b>SDIN</b>	1	<b>Serial Audio Data Input</b> ( <i>Input</i> ) - Input for two's complement serial audio data.
<b>DEM/SCLK</b>	2	<b>De-Emphasis/External Serial Clock Input</b> ( <i>Input</i> ) - used for de-emphasis filter control or external serial clock input.
<b>LRCK</b>	3	<b>Left Right Clock</b> ( <i>Input</i> ) - Determines which channel, Left or Right, is currently active on the serial audio data line.
<b>MCLK</b>	4	<b>Master Clock</b> ( <i>Input</i> ) - Clock source for the delta-sigma modulator and digital filters.
<b>VQ</b>	5	<b>Quiescent Voltage</b> ( <i>Output</i> ) - Filter connection for internal quiescent voltage.
<b>FILT+</b>	6	<b>Positive Voltage Reference</b> ( <i>Output</i> ) - Positive reference voltage for the internal sampling circuits.
<b>AOUTL</b>	7	<b>Left Channel Analog Output</b> ( <i>Output</i> ) - The full scale analog output level is specified in the Analog Characteristics specification table.
<b>GND</b>	8	<b>Ground</b> ( <i>Input</i> ) - ground reference.
<b>VA</b>	9	<b>Analog Power</b> ( <i>Input</i> ) - Positive power for the analog and digital sections.
<b>AOUTR</b>	10	<b>Right Channel Analog Output</b> ( <i>Output</i> ) - The full scale analog output level is specified in the Analog Characteristics specification table.

## 2. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltage and  $T_A = 25^\circ\text{C}$ .)

### SPECIFIED OPERATING CONDITIONS (AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Nom	Max	Units
DC Power Supply	VA	4.75	5.0	5.25	V
		3.14	3.3	3.47	V
Specified Temperature Range	-CZZ -DZZ	$T_A$	-10 -40	- +70 +85	$^\circ\text{C}$ $^\circ\text{C}$

### ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	$I_{in}$	-	$\pm 10$	mA
Digital Input Voltage	$V_{IND}$	-0.3	$VA+0.4$	V
Ambient Operating Temperature (power applied)	$T_{op}$	-55	125	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65	150	$^\circ\text{C}$

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

**DAC ANALOG CHARACTERISTICS** (Full-Scale Output Sine Wave, 997 Hz (Note 1),  
 $F_s = 48/96/192$  kHz; Test load  $R_L = 3$  kΩ,  $C_L = 10$  pF (see Figure 1). Measurement Bandwidth 10 Hz to 20 kHz,  
unless otherwise specified.)

Parameter	5 V Nom			3.3 V Nom			Unit		
	Min	Typ	Max	Min	Typ	Max			
<b>Dynamic Performance for CS4344/5/6/8-CZZ (-10 to 70°C)</b>									
Dynamic Range	18 to 24-Bit	A-weighted	99	105	-	93	99	-	dB
		unweighted	96	102	-	90	96	-	dB
	16-Bit	A-weighted	90	96	-	90	96	-	dB
		unweighted	87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise									
18 to 24-Bit	0 dB	-	-95	-89	-	-95	-89	dB	
	-20 dB	-	-82	-76	-	-76	-70	dB	
	-60 dB	-	-42	-36	-	-36	-30	dB	
16-Bit	0 dB	-	-93	-87	-	-93	-87	dB	
	-20 dB	-	-73	-67	-	-73	-67	dB	
	-60 dB	-	-33	-27	-	-33	-27	dB	
<b>Dynamic Performance for CS4344-DZZ (-40 to 85°C)</b>									
Dynamic Range	18 to 24-Bit	A-weighted	95	105	-	89	99	-	dB
		unweighted	92	102	-	86	96	-	dB
	16-Bit	A-weighted	86	96	-	86	96	-	dB
		unweighted	83	93	-	83	93	-	dB
Total Harmonic Distortion + Noise									
18 to 24-Bit	0 dB	-	-95	-85	-	-95	-85	dB	
	-20 dB	-	-82	-72	-	-76	-66	dB	
	-60 dB	-	-42	-32	-	-36	-26	dB	
16-Bit	0 dB	-	-93	-83	-	-93	-83	dB	
	-20 dB	-	-73	-63	-	-73	-63	dB	
	-60 dB	-	-33	-23	-	-33	-23	dB	

Note: 1. One-half LSB of triangular PDF dither added to data.

## DAC ANALOG CHARACTERISTICS - ALL MODES

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation (1 kHz)		-	100	-	dB
<b>DC Accuracy</b>					
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-	100	-	ppm/°C
<b>Analog Output</b>					
Full Scale Output Voltage		0.640•VA	0.688•VA	0.739•VA	Vpp
Quiescent Voltage	$V_Q$	-	0.5•VA	-	VDC
Max DC Current draw from an AOUT pin	$I_{OUTmax}$	-	10	-	µA
Max Current draw from $V_Q$	$I_{Qmax}$	-	100	-	µA
Max AC-Load Resistance (see Figure 2 on page 8)	$R_L$	-	3	-	kΩ
Max Load Capacitance (see Figure 2)	$C_L$	-	100	-	pF
Output Impedance	$Z_{OUT}$	-	100	-	Ω

## **COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE** (The filter characteristics have been normalized to the sample rate ( $F_s$ ) and can be referenced to the desired sample rate by multiplying the given characteristic by $F_s$ .) (See note 6)

Parameter	Symbol	Min	Typ	Max	Unit
<b>Combined Digital and On-chip Analog Filter Response</b>		<b>Single Speed Mode</b>			
Passband (Note 2) to -0.05 dB corner to -3 dB corner		0 0	- -	.4780 .4996	$F_s$ $F_s$
Frequency Response 10 Hz to 20 kHz		-.01	-	+.08	dB
StopBand		.5465	-	-	$F_s$
StopBand Attenuation (Note 3)		50	-	-	dB
Group Delay	tgd	-	10/ $F_s$	-	s
De-emphasis Error (Note 5) $F_s = 32$ kHz $F_s = 44.1$ kHz $F_s = 48$ kHz		- - -	- - -	+1.5/+0 +.05/-25 -.2/-4	dB dB dB
<b>Combined Digital and On-chip Analog Filter Response</b>		<b>Double Speed Mode</b>			
Passband (Note 2) to -0.1 dB corner to -3 dB corner		0 0	- -	.4650 .4982	$F_s$ $F_s$
Frequency Response 10 Hz to 20 kHz		-.05	-	+.2	dB
StopBand		.5770	-	-	$F_s$
StopBand Attenuation (Note 3)		55	-	-	dB
Group Delay	tgd	-	5/ $F_s$	-	s
<b>Combined Digital and On-chip Analog Filter Response</b>		<b>Quad Speed Mode</b>			
Passband (Note 2) to -0.1 dB corner to -3 dB corner		0 0	- -	0.397 0.476	$F_s$ $F_s$
Frequency Response 10 Hz to 20 kHz		0	-	+0.00004	dB
StopBand		0.7	-	-	$F_s$
StopBand Attenuation (Note 3)		51	-	-	dB
Group Delay	tgd	-	2.5/ $F_s$	-	s

- Notes:
2. Response is clock dependent and will scale with  $F_s$ .
  3. For Single Speed Mode, the Measurement Bandwidth is 0.5465  $F_s$  to 3  $F_s$ .  
 For Double Speed Mode, the Measurement Bandwidth is 0.577  $F_s$  to 1.4  $F_s$ .  
 For Quad Speed Mode, the Measurement Bandwidth is 0.7  $F_s$  to 1  $F_s$ .
  4. Refer to Figure 2.
  5. De-emphasis is available only in Single Speed Mode.
  6. Amplitude vs. Frequency plots of this data are available in "Appendix" on page 21.

## DIGITAL INPUT CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (% of VA)	$V_{IH}$	70%	-	-	V
Low-Level Input Voltage (% of VA)	$V_{IL}$	-	-	30%	V
Input Leakage Current (Note 7)	$I_{in}$	-	-	$\pm 10$	$\mu A$
Input Capacitance		-	8	-	pF

7.  $I_{in}$  for LRCK is  $\pm 20 \mu A$  max.

## POWER AND THERMAL CHARACTERISTICS

Parameters	Symbol	5 V Nom			3.3 V Nom			Units
		Min	Typ	Max	Min	Typ	Max	
<b>Power Supplies</b>								
Power Supply Current normal operation (Note 8)	$I_A$	-	18	25	-	12	16	mA
power-down state (Note 9)	$I_A$	-	60	-	-	40	-	$\mu A$
Power Dissipation normal operation		-	90	125	-	40	53	mW
power-down state (Note 9)		-	0.3	-	-	0.13	-	mW
Package Thermal Resistance	$\theta_{JA}$	-	95	-	-	95	-	$^{\circ}C/Watt$
Power Supply Rejection Ratio (Note 8) (1 kHz)	PSRR	-	60	-	-	60	-	dB
(60 Hz)		-	40	-	-	40	-	dB

- 8. Current consumption increases with increasing FS and increasing MCLK. Typ and Max values are based on highest FS and highest MCLK. Variance between speed modes is small.
- 9. Power down mode is defined when all clock and data lines are held static.
- 10. Valid with the recommended capacitor values on VQ and FILT+ as shown in the typical connection diagram in Section 3.

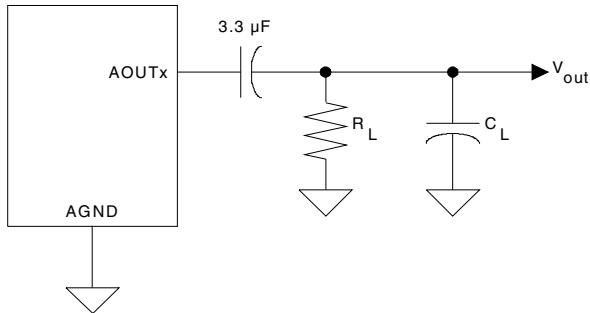


Figure 1. Output Test Load

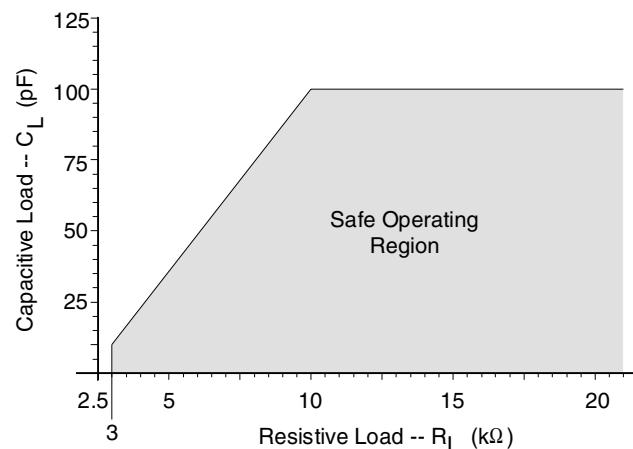


Figure 2. Maximum Loading

## SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		0.512	-	50	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate All MCLK/LRCK ratios combined (Note 11) 256x, 384x, 1024x 256x, 384x 512x, 768x 1152x 128x, 192x 64x, 96x 128x, 192x	Fs	2		200	kHz
		2		50	kHz
		84		134	kHz
		42		67	kHz
		30		34	kHz
		50		100	kHz
		100		200	kHz
		168		200	kHz
<b>External SCLK Mode</b>					
LRCK Duty Cycle (External SCLK only)		45	50	55	%
SCLK Pulse Width Low	t <sub>sclkL</sub>	20	-	-	ns
SCLK Pulse Width High	t <sub>sclkH</sub>	20	-	-	ns
SCLK Duty Cycle		45	50	55	%
SCLK rising to LRCK edge delay	t <sub>sld</sub>	20	-	-	ns
SCLK rising to LRCK edge setup time	t <sub>slds</sub>	20	-	-	ns
SDIN valid to SCLK rising setup time	t <sub>sdlrs</sub>	20	-	-	ns
SCLK rising to SDIN hold time	t <sub>sdh</sub>	20	-	-	ns
<b>Internal SCLK Mode</b>					
LRCK Duty Cycle (Internal SCLK only) (Note 12)		-	50	-	%
SCLK Period (Note 13)	t <sub>sclkW</sub>	$\frac{1}{\text{SCLK}}$	-	-	ns
SCLK rising to LRCK edge	t <sub>sclkr</sub>	-	$\frac{\text{tsclkW}}{2}$	-	μs
SDIN valid to SCLK rising setup time	t <sub>sdlrs</sub>	$\frac{1}{(512)\text{Fs}} + 10$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK = 1152, 1024, 512, 256, 128, or 64	t <sub>sdh</sub>	$\frac{1}{(512)\text{Fs}} + 15$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK = 768, 384, 192, or 96	t <sub>sdh</sub>	$\frac{1}{(384)\text{Fs}} + 15$	-	-	ns

- Notes:
11. Not all sample rates are supported for all clock ratios. See table "Common Clock Frequencies" on page 12 for supported ratio's and frequencies.
  12. In Internal SCLK Mode, the Duty Cycle must be 50% +/- 1/2 MCLK Period.
  13. The SCLK / LRCK ratio may be either 32, 48, 64, or 72. This ratio depends on part type and MCLK/LRCK ratio. (See figures 7-9)

## 6.ORDER INFORMATION:

Model	Temperature	Package	Serial Interface
CS4344-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	16 to 24-bit, I2S
CS4345-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	16 to 24-bit, left justified
CS4346-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	24-bit, right justified
CS4348-CZZ	-10 to +70 °C	10-pin Plastic TSSOP - Lead-Free	16-bit, right justified
CS4344-DZZ	-40 to +85 °C	10-pin Plastic TSSOP - Lead-Free	16 to 24-bit, I2S

## 7.FUNCTIONAL COMPATIBILITY

CS4334-KS ⇒ CS4344-CZZ

CS4335-KS ⇒ CS4345-CZZ

CS4336-KS ⇒ CS4346-CZZ

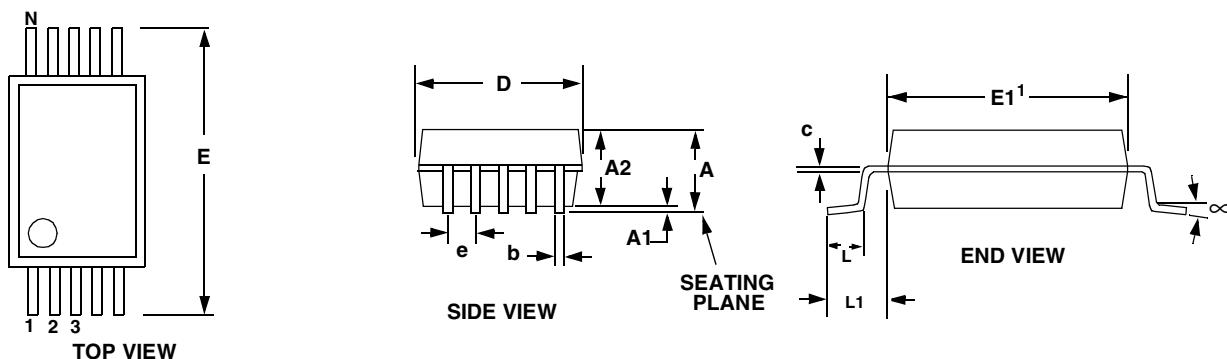
CS4338-KS ⇒ CS4348-CZZ

CS4334-BS ⇒ CS4344-DZZ

CS4334-DS ⇒ CS4344-DZZ

## 8.PACKAGE DIMENSIONS

### 10LD TSSOP (3 mm BODY) PACKAGE DRAWING



DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.0433	--	--	1.10	
A1	0	--	0.0059	0	--	0.15	
A2	0.0295	--	0.0374	0.75	--	0.95	
b	0.0059	--	0.0118	0.15	--	0.30	4, 5
c	0.0031	--	0.0091	0.08	--	0.23	
D	--	0.1181 BSC	--	--	3.00 BSC	--	2
E	--	0.1929 BSC	--	--	4.90 BSC	--	
E1	--	0.1181 BSC	--	--	3.00 BSC	--	3
e	--	0.0197 BSC	--	--	0.50 BSC	--	
L	0.0157	0.0236	0.0315	0.40	0.60	0.80	
L1	--	0.0374 REF	--	--	0.95 REF	--	
$\infty$	0°	--	8°	0°	--	8°	

*Controlling Dimension is Millimeters*

- Notes:
1. Reference document: JEDEC MO-187
  2. D does not include mold flash or protrusions which is 0.15 mm max. per side.
  3. E1 does not include inter-lead flash or protrusions which is 0.15 mm max per side.
  4. Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.
  5. Exceptions to JEDEC dimension.