

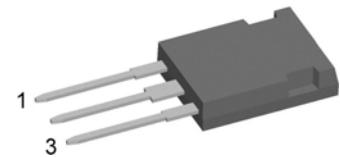
# Thyristor

$V_{RRM}$  = 1600V  
 $I_{TAV}$  = 45A  
 $V_T$  = 1.37V

## Single Thyristor

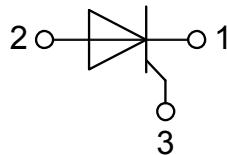
### Part number

CS45-16io1R



Backside: isolated

E72873



### Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

### Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

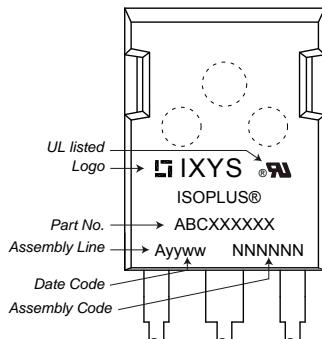
### Package: ISOPLUS247

- Isolation Voltage: 3600V~
- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0
- Soldering pins for PCB mounting
- Backside: DCB ceramic
- Reduced weight
- Advanced power cycling

Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^\circ C$			1700	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^\circ C$			1600	V
$I_{RD}$	reverse current, drain current	$V_{RD} = 1600 \text{ V}$ $V_{RD} = 1600 \text{ V}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = 125^\circ C$		50 3	$\mu A$ mA
$V_T$	forward voltage drop	$I_T = 45 \text{ A}$ $I_T = 90 \text{ A}$ $I_T = 45 \text{ A}$ $I_T = 90 \text{ A}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = 125^\circ C$		1.36 1.73 1.37 1.85	V V V V
$I_{TAV}$	average forward current	$T_C = 80^\circ C$	$T_{VJ} = 150^\circ C$		45	A
$I_{TRMS}$	RMS forward current	180° sine			71	A
$V_{TO}$ $r_T$	threshold voltage slope resistance } for power loss calculation only		$T_{VJ} = 150^\circ C$		0.88 11	V $m\Omega$
$R_{thJC}$	thermal resistance junction to case				0.8	K/W
$R_{thCH}$	thermal resistance case to heatsink			0.25		K/W
$P_{tot}$	total power dissipation		$T_C = 25^\circ C$		150	W
$I_{TSM}$	max. forward surge current	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$ $t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$	$T_{VJ} = 45^\circ C$ $V_R = 0 \text{ V}$ $T_{VJ} = 150^\circ C$ $V_R = 0 \text{ V}$		520 560 440 475	A A A A
$I^2t$	value for fusing	$t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$ $t = 10 \text{ ms}; (50 \text{ Hz}), \text{sine}$ $t = 8,3 \text{ ms}; (60 \text{ Hz}), \text{sine}$	$T_{VJ} = 45^\circ C$ $V_R = 0 \text{ V}$ $T_{VJ} = 150^\circ C$ $V_R = 0 \text{ V}$		1.35 1.31 970 940	kA²s kA²s A²s A²s
$C_J$	junction capacitance	$V_R = 400 \text{ V}$ $f = 1 \text{ MHz}$	$T_{VJ} = 25^\circ C$	22		pF
$P_{GM}$	max. gate power dissipation	$t_p = 30 \mu s$ $t_p = 300 \mu s$	$T_C = 150^\circ C$		10 5 0.5	W W W
$P_{GAV}$	average gate power dissipation					
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 125^\circ C; f = 50 \text{ Hz}$ repetitive, $I_T = 135 \text{ A}$ $t_p = 200 \mu s; di_G/dt = 0.3 \text{ A}/\mu s;$ $I_G = 0.3 \text{ A}; V_D = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 45 \text{ A}$			150	A/ $\mu s$
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V_D = \frac{2}{3} V_{DRM}$ $R_{GK} = \infty$ ; method 1 (linear voltage rise)	$T_{VJ} = 125^\circ C$		1000	V/ $\mu s$
$V_{GT}$	gate trigger voltage	$V_D = 6 \text{ V}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = -40^\circ C$		1.5 1.6	V V
$I_{GT}$	gate trigger current	$V_D = 6 \text{ V}$	$T_{VJ} = 25^\circ C$ $T_{VJ} = -40^\circ C$		80 200	mA mA
$V_{GD}$	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 125^\circ C$		0.2	V
$I_{GD}$	gate non-trigger current				10	mA
$I_L$	latching current	$t_p = 10 \mu s$ $I_G = 0.3 \text{ A}; di_G/dt = 0.3 \text{ A}/\mu s$	$T_{VJ} = 25^\circ C$		150	mA
$I_H$	holding current	$V_D = 6 \text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^\circ C$		100	mA
$t_{gd}$	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$ $I_G = 0.3 \text{ A}; di_G/dt = 0.3 \text{ A}/\mu s$	$T_{VJ} = 25^\circ C$		2	$\mu s$
$t_q$	turn-off time	$V_R = 100 \text{ V}; I_T = 45 \text{ A}; V_D = \frac{2}{3} V_{DRM}$ $T_{VJ} = 150^\circ C$ $di/dt = 15 \text{ A}/\mu s; dv/dt = 20 \text{ V}/\mu s; t_p = 200 \mu s$		150		$\mu s$

Package ISOPLUS247			Ratings		
Symbol	Definition	Conditions	min.	typ.	max.
$I_{RMS}$	RMS current	per terminal			70 A
$T_{stg}$	storage temperature		-55		150 °C
$T_{VJ}$	virtual junction temperature		-40		150 °C
<b>Weight</b>				6	g
$F_c$	mounting force with clip		20		120 N
$d_{Spp/App}$	creepage distance on surface   striking distance through air	terminal to terminal	2.7		mm
$d_{Spb/Apb}$		terminal to backside	4.1		mm
$V_{ISOL}$	isolation voltage	t = 1 second t = 1 minute	3600 50/60 Hz, RMS; $I_{ISOL} \leq 1$ mA	3000	V V

## Product Marking

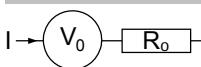


Ordering	Part Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CS45-16io1R	CS45-16io1R	Tube	30	480312

Similar Part	Package	Voltage class
CS45-08io1	TO-247AD (3)	800
CS45-12io1	TO-247AD (3)	1200
CS45-16io1	TO-247AD (3)	1600

## Equivalent Circuits for Simulation

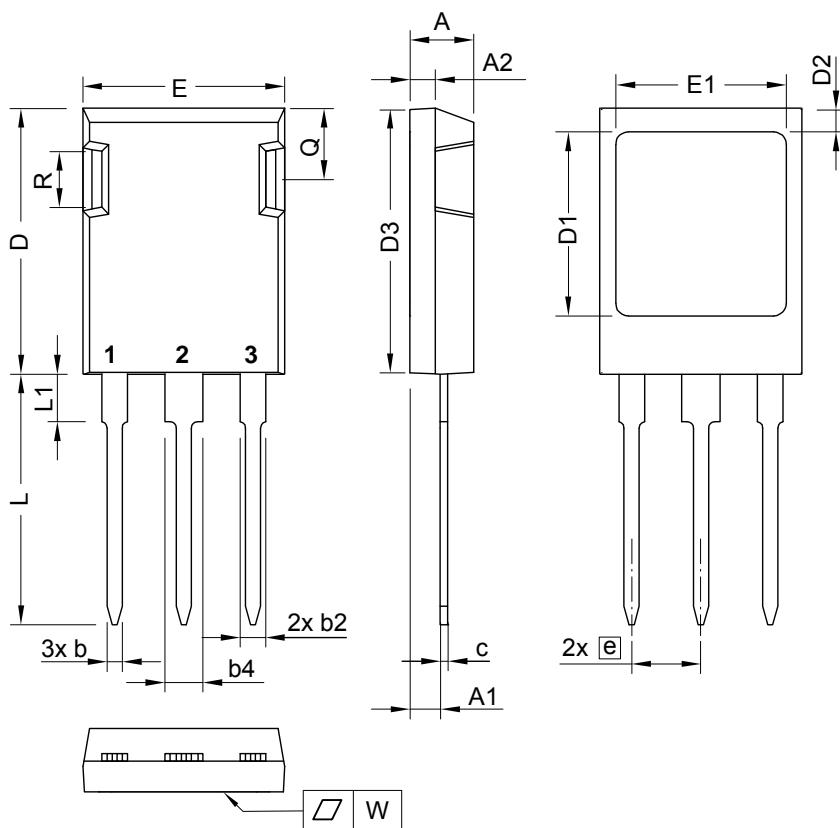
\* on die level

 $T_{VJ} = 150^\circ\text{C}$ 

Thyristor

$V_{0\max}$  threshold voltage 0.88 V  
 $R_{0\max}$  slope resistance \* 8.5 mΩ

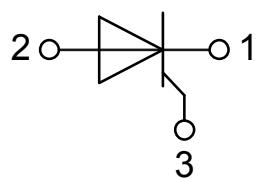
## Outlines ISOPLUS247



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.83	5.21	0.190	0.205
A1	2.29	2.54	0.090	0.100
A2	1.91	2.16	0.075	0.085
b	1.14	1.40	0.045	0.055
b2	1.91	2.20	0.075	0.087
b4	2.92	3.24	0.115	0.128
c	0.61	0.83	0.024	0.033
D	20.80	21.34	0.819	0.840
D1	15.75	16.26	0.620	0.640
D2	1.65	2.15	0.065	0.085
D3	20.30	20.70	0.799	0.815
E	15.75	16.13	0.620	0.635
E1	13.21	13.72	0.520	0.540
e	5.45	BSC	0.215	BSC
L	19.81	20.60	0.780	0.811
L1	3.81	4.38	0.150	0.172
Q	5.59	6.20	0.220	0.244
R	4.25	5.50	0.167	0.217
W	-	0.10	-	0.004

Die konvexe Form des Substrates ist typ. < 0.04 mm über der Kunststoffoberfläche der Bauteilunterseite  
*The convex bow of substrate is typ. < 0.04 mm over plastic surface level of device bottom side*

Die Gehäuseabmessungen entsprechen dem Typ TO-247 AD gemäß JEDEC außer Schraubloch und L<sub>max</sub>.  
*This drawing will meet all dimensions requirement of JEDEC outline TO-247 AD except screw hole and except L<sub>max</sub>.*



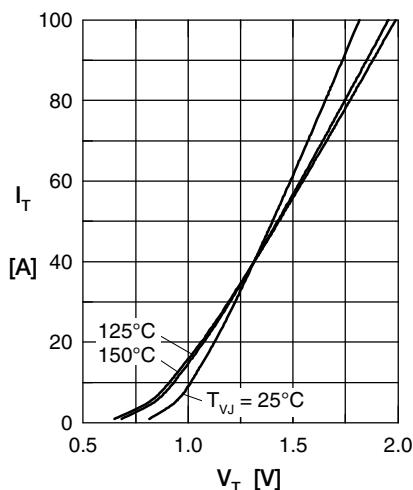
**Thyristor**

Fig. 1 Forward characteristics

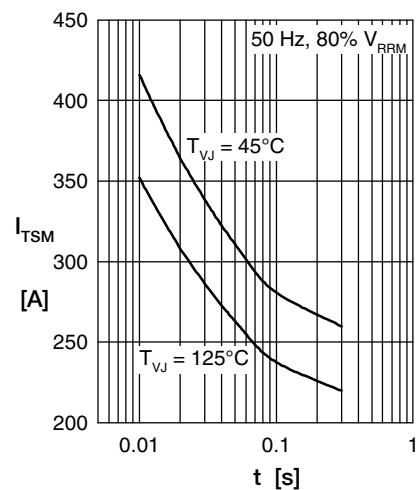


Fig. 2 Surge overload current

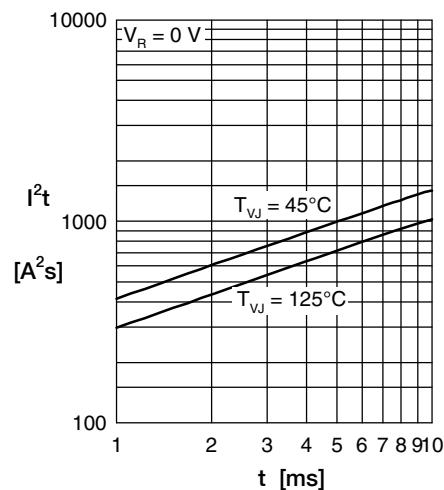
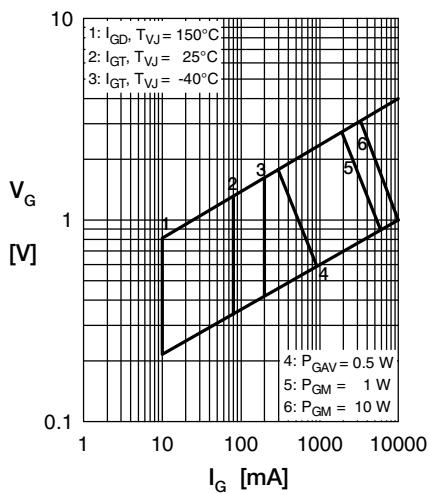
Fig. 3  $I^2t$  versus time (1-10 ms)

Fig. 4 Gate trigger characteristics

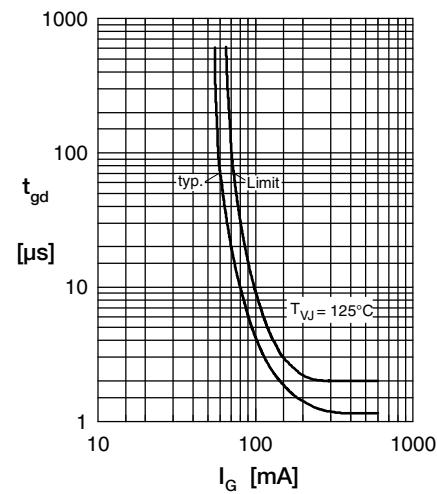


Fig. 5 Gate controlled delay time

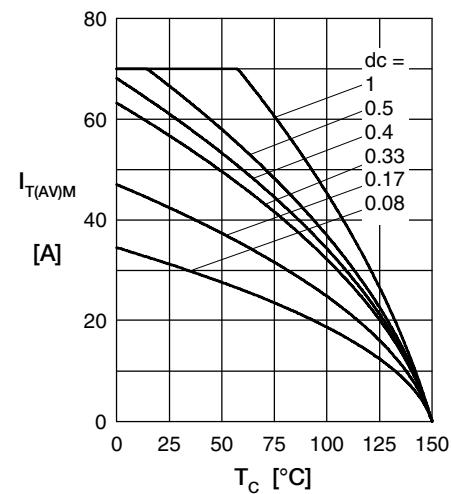


Fig. 6 Max. forward current at case temperature

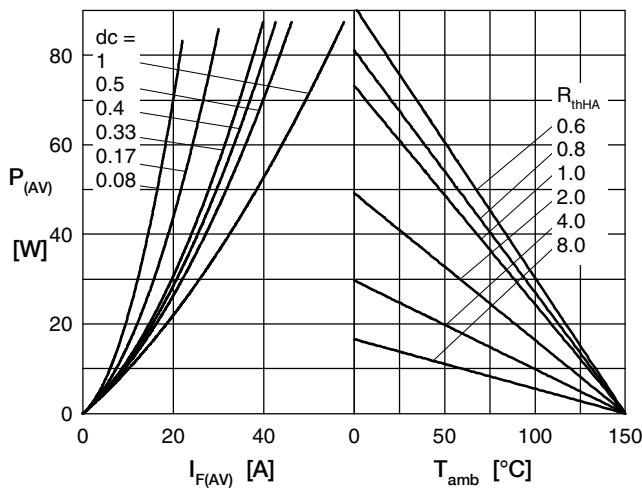
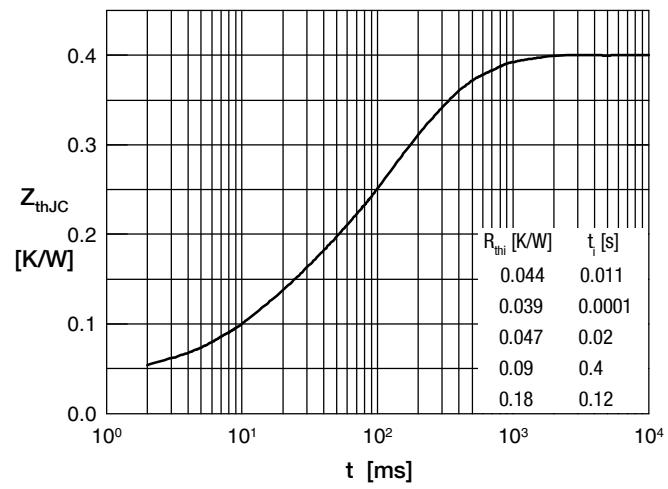
Fig. 7a Power dissipation versus direct output current  
Fig. 7b and ambient temperature

Fig. 8 Transient thermal impedance