

# **Dual High-Voltage Isolated MOSFET Driver**

#### **Features**

- ±400V Input to Output Isolation
- · ±700V Isolation between Outputs
- · No External Voltage Supply Required
- · Dual Isolated Output Drivers
- · Internal and External Clock Options

### **Applications**

- Telecommunications
- Modems
- Solid-state Relays
- · High-side Switches
- · High-end Audio Switches
- Avionics
- · Automatic Test Equipment

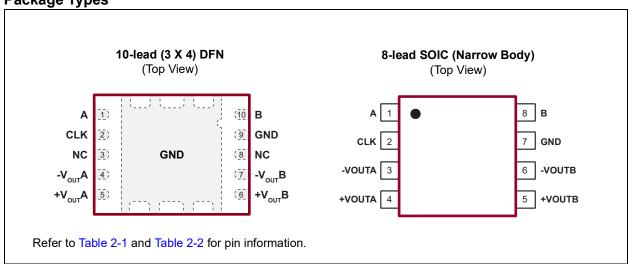
#### **General Description**

HT0440 is a dual high-voltage isolated MOSFET driver that uses HVCMOS technology. It is designed to drive discrete MOSFETs configured as bidirectional or unidirectional switches. In addition, it can drive N-channel MOSFETs as high-side switches up to 400V. The HT0440 generates two independent DC-isolated voltages to the outputs  $V_{OUT}A$  and  $V_{OUT}B$  when logic inputs A and B are at logic high.

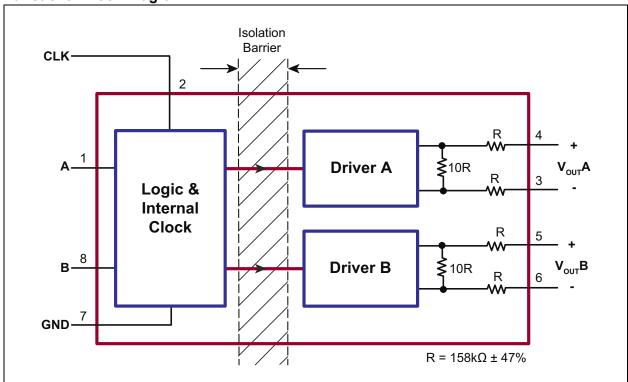
The internal clock of the HT0440 can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be customized to meet specific needs. The CLK pin should be connected to ground when not in use. The HT0440 does not require any external power supplies. The internal supply voltage is provided by either of the two logic inputs, A or B, when these inputs are at logic high.

For detailed circuit application information, please refer to application note, AN-D26 High-Voltage Isolated MOSFET Driver.

## **Package Types**



# **Functional Block Diagram**



### 1.0 ELECTRICAL CHARACTERISTICS

## **Absolute Maximum Ratings†**

Input to Output Isolation Voltage, V <sub>ISO</sub>	±400V
Logic Input Voltage, V <sub>A</sub> , V <sub>B</sub>	
Maximum Junction Temperature, T <sub>.IMAX</sub>	
Storage Temperature, T <sub>S</sub>	
Maximum Junction Temperature, T <sub>.1</sub>	

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions
External Clock Frequency	CLK	0.5	_	2	MHz	
Clock Input High Voltage	V <sub>IHCLK</sub>	3.15	_	5.5	V	
Clock Input Low Voltage	V <sub>ILCLK</sub>	0	_	0.5	V	
Logic Input High Voltage	V <sub>IH</sub>	3.15	_	5.5	V	
Logic Input Low Voltage	V <sub>IL</sub>	0	_	0.5	V	
Operating Temperature	T <sub>A</sub>	-40	_	+85	°C	

### DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T <sub>A</sub> =	<b>Electrical Specifications</b> : T <sub>A</sub> = 25°C unless otherwise indicated.											
Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions						
		1	1	300	μA	V <sub>A</sub> = 3.5V, V <sub>B</sub> = 3.5V, CLK = 0V						
				500	μΑ	$V_A = 3.5V$ , $V_B = 3.5V$ , CLK = 500 kHz						
Total Logic High Input Current	$I_{HA} + I_{HB}$			2	mA	$V_A = 3.5V, V_B = 3.5V, CLK = 2 MHz$						
		_	_	1	mA	$V_A = 5.5V, V_B = 5.5V, CLK = 0V$						
		_	_	2	mA	$V_A = 5.5V$ , $V_B = 5.5V$ , CLK = 500 kHz						
		6			V	$V_A = 3.15V$ , $V_B = 3.15V$ , CLK = 0V, No load						
	V <sub>OUTA</sub> , V <sub>OUTB</sub>	5			V	$V_A = 3.15V$ , $V_B = 3.15V$ , CLK = 500 kHz, No load						
Output Voltage		6		_	V	$V_A = 3.15V, V_B = 3.15V,$ CLK = 2 MHz, No load						
		10	ı		V	$V_A = 4.5V, V_B = 4.5V,$ CLK = 0V, No load						
		8	ı		V	$V_A = 4.5V, V_B = 4.5V,$ CLK = 500 kHz, No load						
Logic Low Input A Current	I <sub>ILA</sub>		_	10	μA	$V_A = 0.5V$ , $V_B = High$						
Logic Low Input B Current	$I_{ILB}$			10	μA	$V_A$ = High, $V_B$ = 0.5V						
Quiescent Current	I <sub>ILQ</sub>	_	_	10	μA	$V_A = 0.5V, V_B = 0.5V$						
Input to Output Isolation Voltage	V <sub>ISO</sub>	±400		_	V							
Output to Output Isolation Voltage	V <sub>CISO</sub>	±700	_	_	٧							

## **AC ELECTRICAL CHARACTERISTICS**

Electrical Specifications: T <sub>A</sub> = 25°C unless otherwise indicated.									
Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions			
Turn-on Delay Time	t <sub>d(ON)</sub>	_	_	50	μs				
Rise Time	t <sub>r</sub>	_	_	650	μs	See Timing Waveforms and Test Circuit. CLK = 0V, CL = 600 pF			
Turn-off Delay Time	t <sub>d(OFF)</sub>	_	_	150	μs				
Fall Time	t <sub>f</sub>	_	_	3	ms	•			

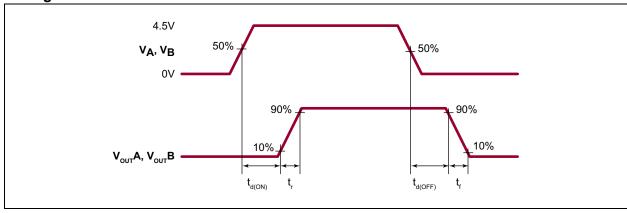
## **TEMPERATURE SPECIFICATIONS**

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions				
TEMPERATURE RANGES										
Junction Temperature	$T_J$	_	_	+125	°C					
Operating Temperature	T <sub>A</sub>	-40	_	+85	°C					
Storage Temperature	T <sub>S</sub>	-55	_	+150	°C					
PACKAGE THERMAL RESISTANC	ES									
10-lead DFN	$\theta_{\sf JA}$	_	40	_	°C/W					
8-lead SOIC (Narrow Body)	$\theta_{JA}$	_	101	_	°C/W					

### TABLE 1-1: TRUTH TABLE

Α	В	CLK	V <sub>OUT</sub> A	V <sub>OUT</sub> B	Internal Clock	
0	0	0	OFF	OFF	OFF	
0		0	OFF	ON	ON	
」	0	0	ON	OFF	ON	
1	1	0	ON	ON	ON	
0	0	CLK	OFF	OFF	OFF	
0		CLK	OFF	ON	OFF	
」	0	CLK	ON	OFF	OFF	
1	1	CLK	ON	ON	OFF	

# **Timing Waveforms**



## 2.0 PIN DESCRIPTION

The details on the pins of HT0440 are listed in Table 2-1 and Table 2-2. Refer to **Package Types** for the location of pins.

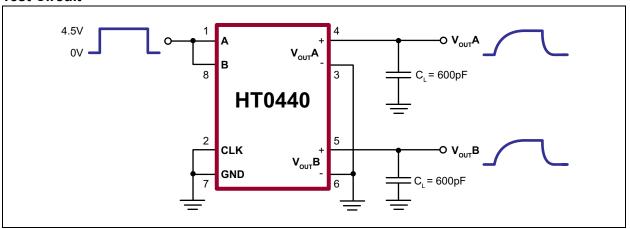
TABLE 2-1: 10-LEAD DFN PIN TABLE

Pin Number	Pin Name	Description					
1	Α	Logic input for controlling Output A.					
2	CLK	Clock input for the IC. Connect to GND to use internal clock. Connect to external clock signal to use external Clock. External clock frequency should be between 500 kHz and 2 MHz.					
3	NC	No connect pin. Leave unconnected.					
4	-VOUTA	Channel A isolated output. +VOUTA is the positive terminal and –VOUTA is the					
5	+VOUTA	negative terminal. Connect to the load.					
6	+VOUTB	Channel B isolated output. +VOUTB is the positive terminal and –VOUTB is the					
7	-VOUTB	negative terminal. Connect to the load.					
8	NC	No connect pin. Leave unconnected.					
9	GND	GND connection. Connect to GND of the input digital signals.					
10	В	Logic input for controlling Output B.					
Thermal pad	GND	GND connection. Connect to GND of the input digital signals.					

TABLE 2-2: 8-LEAD SOIC PIN TABLE

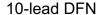
Pin Number	Pin Name	Description
1	А	Logic input for controlling Output A.
2	CLK	Clock input for the IC. Connect to GND to use internal clock. Connect to external clock signal to use external Clock. External clock frequency should be between 500 kHz and 2 MHz.
3	-VOUTA	Channel A isolated output. +VOUTA is the positive terminal and –VOUTA is the
4	+VOUTA	negative terminal. Connect to the load.
5	+VOUTB	Channel B isolated output. +VOUTB is the positive terminal and –VOUTB is the
6	-VOUTB	negative terminal. Connect to the load.
7	GND	GND connection. Connect to GND of the input digital signals.
8	В	Logic input for controlling Output B.

# **Test Circuit**



#### 3.0 PACKAGING INFORMATION

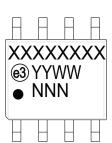
## 3.1 Package Marking Information





### Example

8-lead SOIC



## Example



Legend: XX...X Product Code or Customer-specific information

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code

e3 Pb-free JEDEC® designator for Matte Tin (Sn)

This package is Pb-free. The Pb-free JEDEC designator (e3)

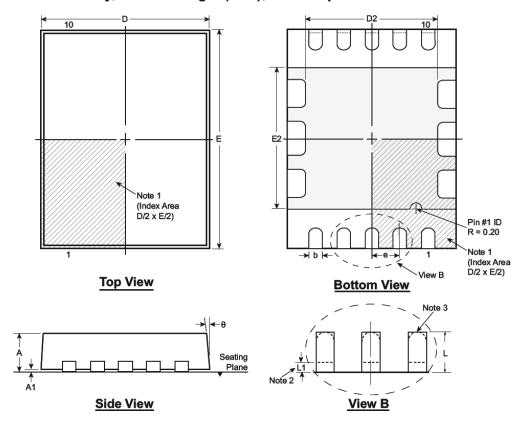
can be found on the outer packaging for this package.

Note:

In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

# 10-Lead DFN Package Outline (K6)

3.00x4.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

#### Notes:

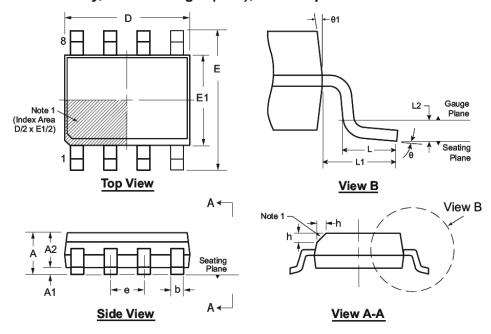
- 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present. The inner tip of the lead may be either rounded or square.

Symb	ol	Α	A1	b	D	D2	E	<b>E</b> 2	е	L	L1	θ
	MIN	0.80	0.00	0.18	2.95	2.20	3.95	2.50		0.30	0.00	<b>0</b> °
Dimension (mm)	NOM	0.90	0.02	0.25	3.00	2.35	4.00	2.65	0.50 BSC	0.40	-	-
()	MAX	1.00	0.05	0.30	3.05	2.45	4.05	2.75	500	0.50	0.15	14º

Drawings not to scale.

# 8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

#### Note:

 This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbo	ı	Α	A1	A2	b	D	E	<b>E</b> 1	е	h	L	L1	L2	θ	θ1
	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*		0.25	0.40			<b>0</b> o	<b>5</b> °
Dimension (mm)	NOM	-	-	-	-	4.90	6.00	3.90	1.27 BSC	-	-	1.04 REF	0.25 BSC	-	-
()	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27	į		8º	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

Drawings are not to scale.

<sup>\*</sup> This dimension is not specified in the JEDEC drawing.

## **APPENDIX A: REVISION HISTORY**

## **Revision A (September 2022)**

- Converted Supertex Doc# DSFP-HT440 to Microchip DS20005606A.
- Made minor text changes throughout the document.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX		. x . x	Exa	amples:	
Device			Environmental Media Type	a)	HT0440K6-G:	Dual High-Voltage Isolated MOSFET Driver, 10-lead (3 x 4) DFN Package, 3300/Reel
Device:	HT0440	=	Dual High-Voltage Isolated MOSFET Driver	b)	HT0440LG-G:	Dual High-Voltage Isolated MOSFET Driver, 8-lead SOIC Package, 3300/ Reel
Package:	K6 LG	=	10-lead (3 x 4) DFN 8-lead SOIC			
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package			
Media Type:	(blank)	=	3300/Reel for an KG Package 3300/Reel for an LG Package			

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