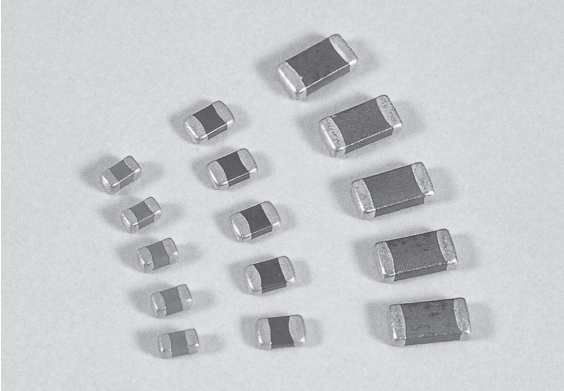
MULTI LAYER CERAMIC CHIP CAPACITOR



FEATURES

Nickel barrier end terminations to improve solderability.
Multilayer block structure provides higher reliability.
A wide range of capacitance values available in standard case sizes.

APPLICATIONS

General Electronic Devices.

PRODUCT IDENTIFICATION

M	0603	X	103	K	050	T
①	②	③	④	⑤	⑥	⑦

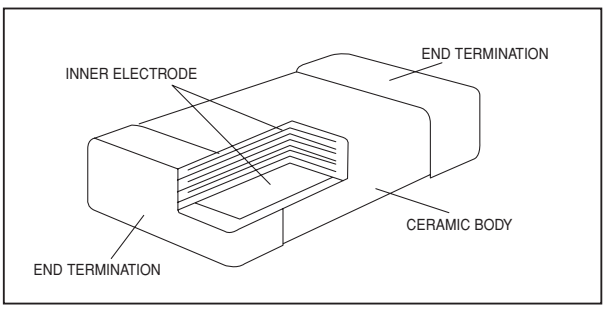
① STANDARD TYPE MLCC

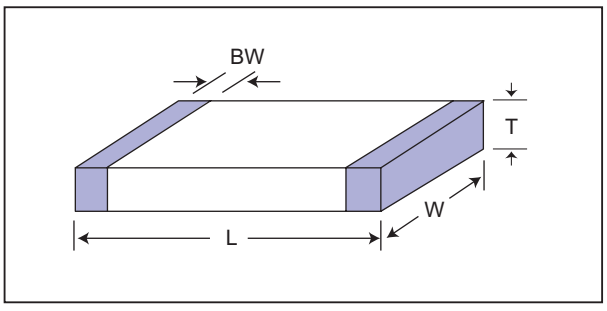
② DIMENSION

Unit : mm

Code	LWT(max)BW			
0201	0.60	0.030.30	0.030.330.15	0.05
0402	1.00	0.050.50	0.050.550.25	0.10
0603	1.60	0.100.80	0.100.950.35	0.15
0805	2.00	0.201.25	0.201.400.45	0.25
1206	3.20	0.301.60	0.201.800.50	0.20
1210	3.20	0.302.50	0.202.700.60	0.30
1808	4.50	0.402.00	0.302.200.80	0.40
1812	4.50	0.403.20	0.303.300.80	0.40
2220	5.70	0.405.00	0.403.301.00	0.50

STRUCTURE





PRODUCT IDENTIFICATION

③ TEMPERATURE CHARACTERISTIC

Code	EIA Code	Temperature Coefficient (ppm/℃)	Capacitance Change (△C : %)	Operating Temperature Range
N	NP0(C0G)	0±30		−55～+125℃
B	X5R		±15%	−55～+85℃
X	X7R		±15%	−55～+125℃
Y	Y5V		+22～−82%	−30～+85℃
E	Y5U		+22～−56%	−30～+85℃
Z	Z5U		+22～−56%	+10～+85℃

④ CAPACITANCE

Code	Capacitance (pF)	Code	Capacitance (pF)
OR5	0.5	101	100
010	1	104	100,000 (100nF)
100	10	106	10,000,000 (10uF)

⑤ CAPACITANCE TOLERANCE

Code	B	C	D	F	G
Tolerance	±0.10pF	±0.25pF	±0.50pF	±1.0%	±2.0%
Code	H	J	K	M	Z
Tolerance	±3.0%	±5.0%	±10%	±20%	−20～+80%

⑥ RATED VOLTAGE

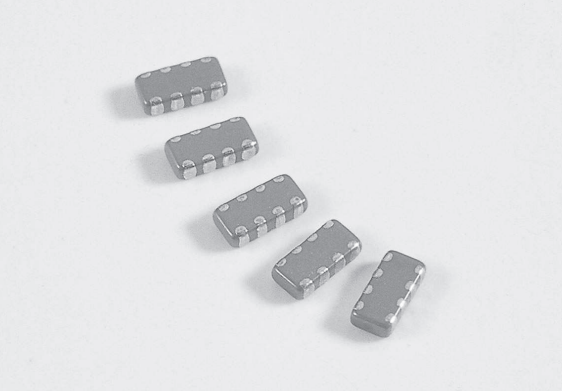
Code	007	010	016	025	050
Rated Voltage	6.3V	10V	16V	25V	50V

⑦ PACKAGING

Code	Description Of The Code
T	Tape & reel
B	Bulk

MULTI LAYER CERAMIC CHIP CAPACITOR

Temperature Characteristic	Size	Voltage	Capacitance Range (pF)
CLASS I NPO	0201	16	100
		25	100
	0402	25	330
		50	180
	0603	50	1,000
	0805	50	4,700
	1206	50	10,000
CLASS II X7R/X5R	0201 (0603)	6.3	1,000 – 100,000
		10	1,000 – 6,800
		16	100 – 1,000
	0402 (1005)	10	100 – 100,000
		16	100 – 100,000
		25	100 – 22,000
		50	100 – 10,000
	0603 (1608)	6.3	330,000 – 2,200,000
		10	100 – 1,000,000
		16	100 – 220,000
		25	100 – 100,000
		50	100 – 22,000
	0805 (2012)	6.3	1,500,000 – 4,700,000
		10	100 – 3,300,000
		16	100 – 1,000,000
		25	100 – 470,000
		50	100 – 220,000
	1206 (3216)	6.3	1,000 – 22,000,000
		10	1,000 – 22,000,000
		16	1,000 – 10,000,000
		25	1,000 – 2,200,000
		50	1,000 – 470,000
	1210 (3225)	10	220,000 – 22,000,000
		16	220,000 – 10,000,000
		25	220,000 – 10,000,000
		50	220,000 – 2,200,000
	1812 (4532)	10	220,000 – 47,000,000
		16	220,000 – 33,000,000
		25	220,000 – 22,000,000
		50	220,000 – 3,300,000
	2220 (5750)	6.3	2,200,000 – 100,000,000
		10	10,000,000 – 47,000,000
		16	10,000,000 – 22,000,000
		25	4,700,000 – 10,000,000
		50	100,000 – 4,700,000
CLASS II Y5V	0402 (1005)	16	2,200 – 220,000
		25	2,200 – 47,000
		50	2,200 – 10,000
	0603 (1608)	6.3	1,000 – 2,200,000
		10	1,000 – 1,000,000
		16	1,000 – 1,000,000
		25	1,000 – 330,000
		50	1,000 – 100,000
	0805 (2012)	6.3	1,000 – 10,000,000
		10	1,000 – 10,000,000
		16	1,000 – 4,700,000
		25	1,000 – 2,200,000
		50	1,000 – 220,000
	1206 (3216)	10	1,000 – 22,000,000
		16	1,000 – 10,000,000
		25	1,000 – 4,700,000
		50	1,000 – 1,000,000
	1210 (3225)	10	220,000 – 22,000,000
		16	220,000 – 22,000,000
		25	220,000 – 10,000,000
		50	220,000 – 4,700,000
	1812 (4532)	10	220,000 – 47,000,000
		16	220,000 – 22,000,000
		25	220,000 – 10,000,000
	2220 (5750)	10	220,000 – 100,000,000
		16	220,000 – 47,000,000
		25	220,000 – 33,000,000
		31.5	220,000 – 22,000,000
		50	220,000 – 10,000,000



FEATURES

Reduction in required real estate(more than 50)
Reduced Cost,Space and Time for placement on PCB
Reduction in number of solder joints
Easier PCB design
Reduced waste from tape and reel packaging process
It protect EMI bypassing digital signal line noise

APPLICATIONS

Mother Board, Notebook, Electionic Devices etc...

PRODUCT IDENTIFICATION

MA	6	N	1H	100	K	T
①	②	③	④	⑤	⑥	⑦

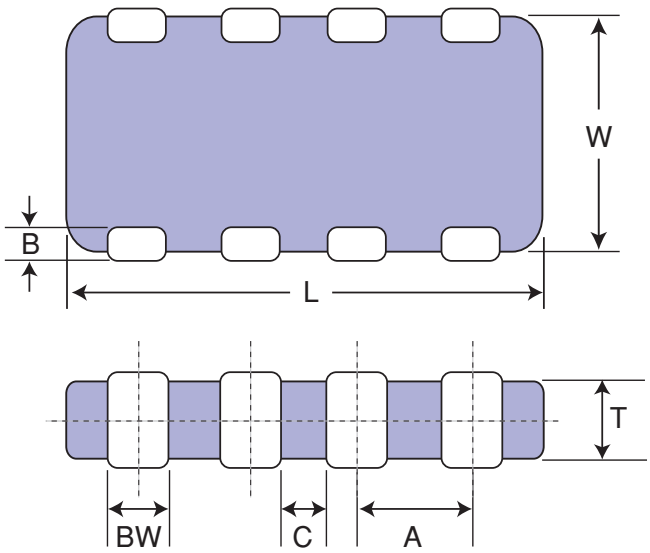
① CAPACITOR ARRAY TYPE MLCC

② DIMENSION

DIMENSION

(Unit : mm)

Code	EIA Code	L	W	T	B	BW	A	C
5	0805	2.0±0.15	1.25±0.15	1.0MAX	0.25±0.1	0.25±0.1	0.5±0.1	0.25±0.1
6	1206	3.2±0.2	1.6±0.2	1.35MAX	0.3±0.2	0.4±0.2	0.8±0.1	0.4±0.2



PRODUCT IDENTIFICATION

③ TEMPERATURE CHARACTERISTIC

Code	EIA Code	Temperature Coefficient (ppm / ℃)	Capacitance Change (△C : %)	Operating Temperature Range
N	NP0(C0G)	0±30		−55～+125℃
X	X7R		±15%	−55～+125℃
Y	Y5V		+22～−82%	−30～+85℃

④ RATED VOLTAGE

Code	0J	1A	1C	1E	1H
Rated Voltage	6.3V	10V	16V	25V	50V

⑤ CAPACITANCE

Code	Capacitance (pF)	Code	Capacitance (pF)
OR5	0.5	101	100
010	1	102	1000 (1nF)
100	10	103	10000 (10nF)

⑥ CAPACITANCE TOLERANCE

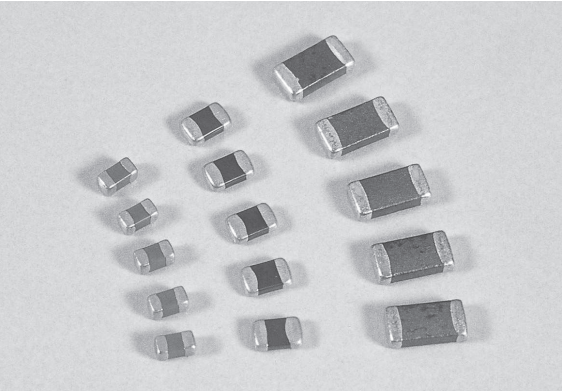
Code	J	K	M	Z
Tolerance	±5%	±10%	±20%	−20～+80%

⑦ PACKAGING

Code	Description Of The Code
T	Tape & reel
B	Bulk

Temperature Characteristic	Type	Rated Voltage	Capacitance Range (pF) 050 100 101 102 103 104 105 106
NP0 (C0G)	(0805) 1206 4 cap	50	10 – 470
X7R		16	470 – 100,000
		25	470 – 47,000
		50	470 – 22,000
Y5V		16	10,000 – 220,000
		25	10,000 – 100,000
		50	10,000 – 47,000

HIGH VOLTAGE MULTILAYER CERAMIC CHIP CAPACITOR



FEATURES

Small case size with high rated voltage, ranging voltage from 100V to 3000V.

These device are compliant with TUV.

APPLICATIONS

General telephone exechange.

Wireless and telecommunication.

Power device.

PRODUCT IDENTIFICATION

MH	1808	X	102	K	202	T
①	②	③	④	⑤	⑥	⑦

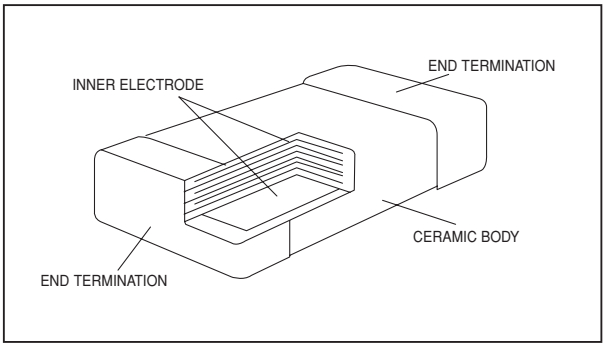
① HIGH VOLTAGE TYPE MLCC

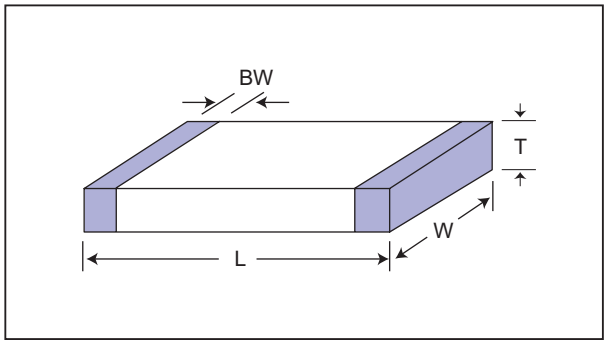
② DIMENSION

Unit : mm

Code	LWT(max)	BW		
0603	1.60 0.10	0.80 0.10	0.95 0.35	0.15
0805	2.00 0.20	1.25 0.20	1.40 0.45	0.25
1206	3.20 0.30	1.60 0.20	1.80 0.50	0.20
1210	3.20 0.30	2.50 0.20	2.70 0.60	0.30
1808	4.50 0.40	2.00 0.20	2.20 0.80	0.40
1812	4.50 0.40	3.20 0.30	3.30 0.80	0.40
2220	5.70 0.40	5.00 0.40	3.30 1.00	0.50

STRUCTURE





PRODUCT IDENTIFICATION

③ TEMPERATURE CHARACTERISTIC

Code	EIA Code	Temperature Coefficient (ppm / ℃)	Capacitance Change (△C : %)	Operating Temperature Range
N	NP0(C0G)	0±30		−55～+125℃
B	X5R		±15%	−55～+85℃
X	X7R		±15%	−55～+125℃
Y	Y5V		+22～−82%	−30～+85℃
E	Y5U		+22～−56%	−30～+85℃
Z	Z5U		+22～−56%	+10～+85℃

④ CAPACITANCE

Code	Capacitance (pF)	Code	Capacitance (pF)
OR5	0.5	101	100
010	1	102	1000 (1nF)
100	10	103	10000 (10nF)

⑤ CAPACITANCE TOLERANCE

Code	B	C	D	F	G
Tolerance	±0.10pF	±0.25pF	±0.50pF	±1.0%	±2.0%
Code	H	J	K	M	Z
Tolerance	±3.0%	±5.0%	±10%	±20%	−20～+80%

⑥ RATED VOLTAGE

Code	101	251	501	102	202	302
Rated Voltage	100V	250V	500V	1000V	2000V	3000V

⑦ PACKAGING

Code	Description Of The Code
T	Tape & reel
B	Bulk

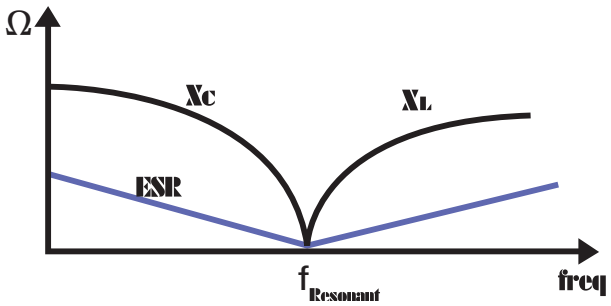
HIGH VOLTAGE MULTILAYER CERAMIC CHIP CAPACITOR

Temperature Characteristic	Size	Voltage	Capacitance Range (pF)
CLASS I NPO	0603	100	680
	0805	100	1,200
		250	1,000
		500	470
	1206	250	22 – 4,700
		500	22 – 2,200
		1000	10 – 470
		2000	10 – 470
	1210	250	10 – 2,200
	1808	1000	5 – 1,000
		2000	5 – 1,000
		3000	5 – 1,000
	1812	1000	5 – 4,700
		2000	5 – 3,300
		3000	5 – 1,500
CLASS II X7R/X5R	0603	100	100 – 4,700
	0805	100	100 – 22,000
		250	100 – 22,000
		500	100 – 4,700
	1206	100	680 – 220,000
		250	680 – 100,000
		500	680 – 47,000
		1000	680 – 10,000
		2000	180 – 4,700
	1210	100	1,000 – 470,000
		250	1,000 – 100,000
		500	1,000 – 100,000
	1808	100	2,200 – 68,000
		250	2,200 – 68,000
		500	2,200 – 68,000
		1000	2,700 – 22,000
		2000	150 – 6,200
		3000	150 – 3,300
	1812	100	10,000 – 1,500,000
		250	10,000 – 470,000
		500	10,000 – 160,000
		1000	470 – 47,000
		2000	470 – 22,000
		3000	470 – 4,700
	2220	1000	3,300 – 82,000
		2000	2,200 – 47,000
		3000	1,200 – 9,100
CLASS II Y5V /Y5U/ Z5U	1210	100	1,000,000 – 1,500,000
	1812	100	10,000 – 470,000
		250	10,000 – 470,000
	2220	100	10,000 – 1,500,000
		250	10,000 – 1,000,000

DIELECTRIC MATERIAL

Material	Tolerance	Characteristics	Application
NPO (COG)	1)B,C,D,F,G 2)J,K prefered	Class I Low K dielectric: extremely stabel in capacitance regardless of time and temperature change. With low dielectric loss and small tolerance on nominal capacitance.	Precision timing circuits, high frequency noise filtering impedance matching, ESD Limiting.
X7R	1)J±5% 2)K,M Prefered	Class II middie K dielectric: allowing higher capacitance than class I dielectric in less stable frequency, voltage, and temperature condition.	Noise filtering, frequency discrimination, by-pass and decoupling in radio receivers, audio tone, and computer servo system.
Z5U And Y5V	1)k±10% 2)M, Z Prefered	Class II High K dielectric: allowing high capacitance density as a Replacement of tantalum, aluminum electrotytic capacitor.	Low frequency noise by-pass and high speed power decoupling application.

Frequency Response model of a Capacitor



$$\text{Resonant Frequency, } fc = \frac{1}{2\pi\sqrt{LC}}$$

$$|Z| = \sqrt{ESR^2 + (Xc - XL)^2}$$

$$Xc = \frac{1}{2\pi fC}$$

$$XL = 2\pi fL$$

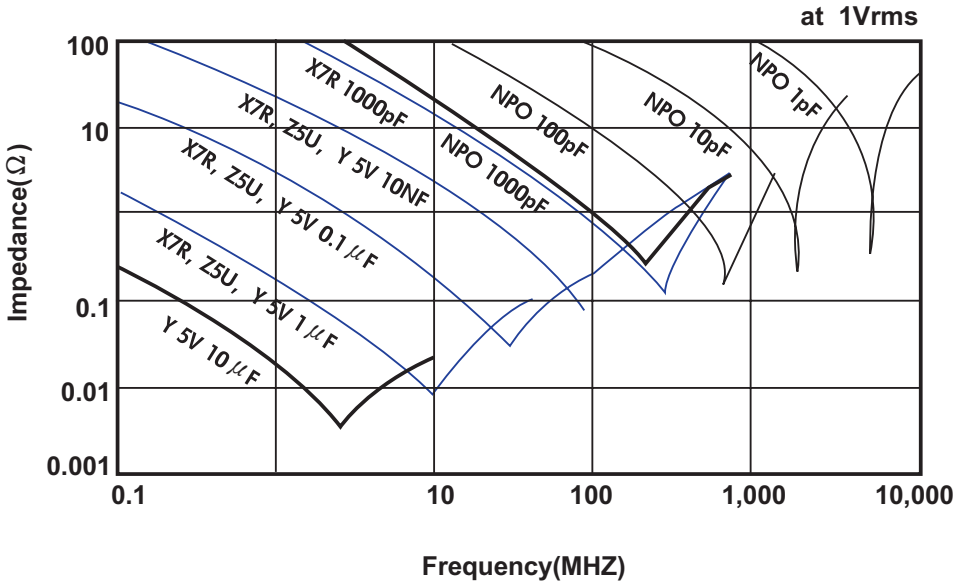
$$C = \frac{0.224KA}{t}$$

C= capacitance (Farads)
K= Dielectric constant
A= Area in square inches
t= Thickness of dielectric

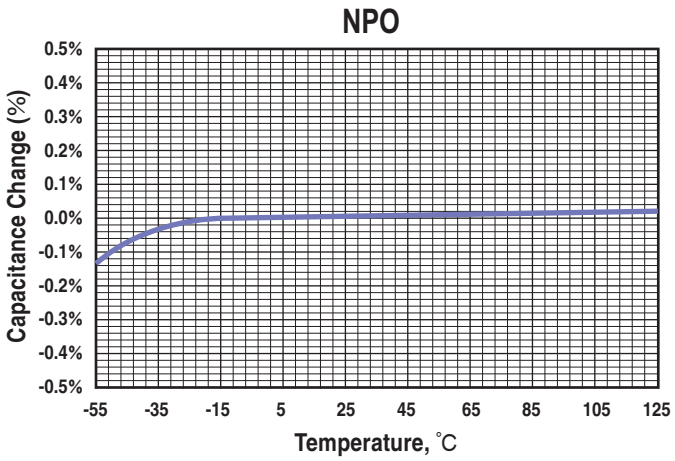
0.224=conversion constant
0.0884 for metric system, cm

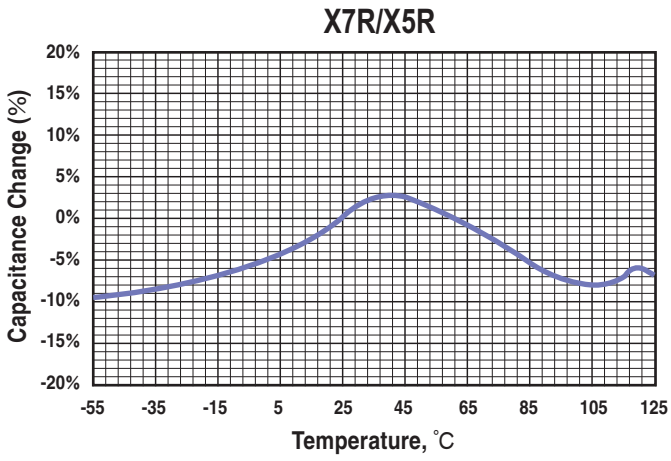
When 1) Working frequency = SRF of a capacitor
Xc - XL = O, |Z| ≈ ESR
2) Working frequency < SRF
|Z| dominated by Xc
3) Working frequency > SRF
|Z| dominated by XL

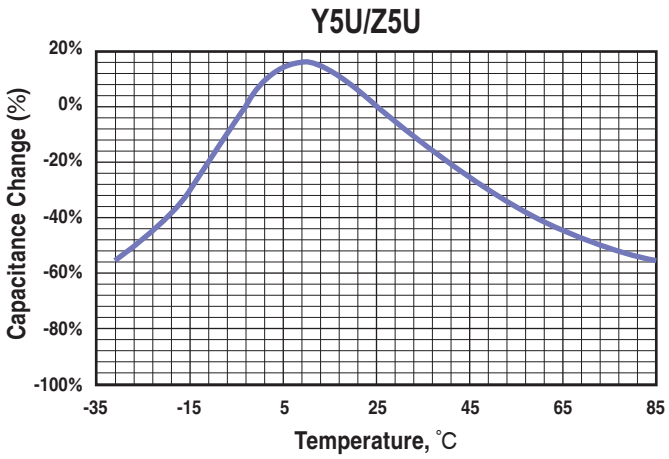
Typical NPO, X7R, Z5U, Y5V Frequency Response

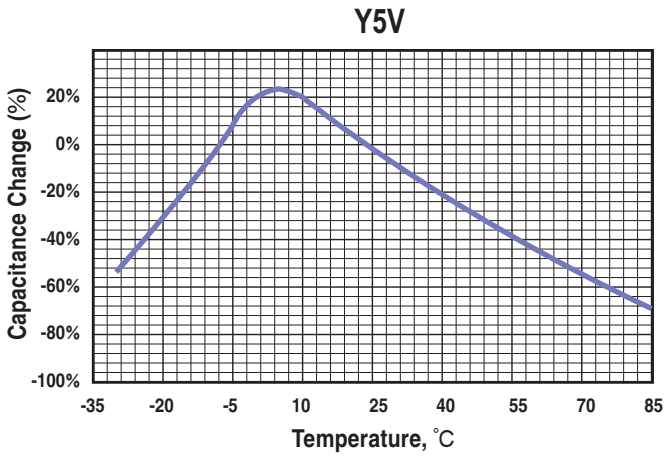


Tolerance Of Temperature Coefficient



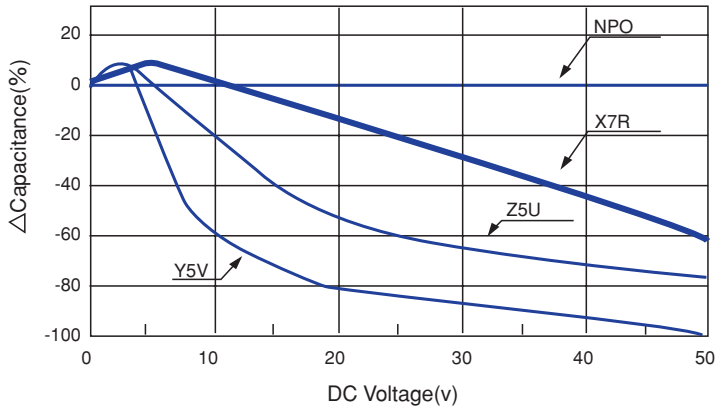




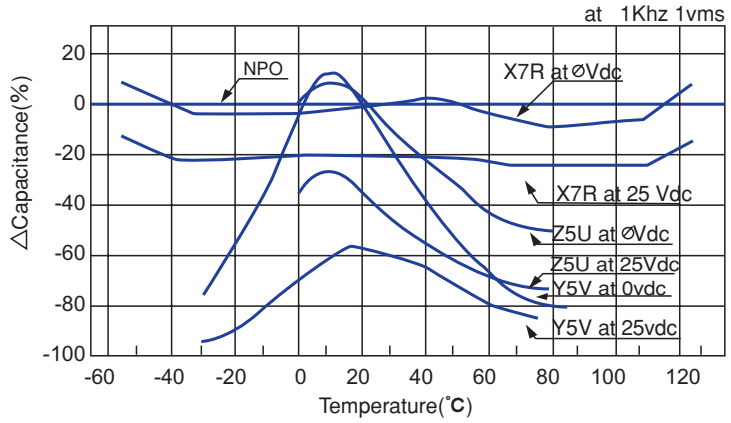


Typical NPO, X7R, Y5V DC bias vs. Capacitance

For temperature compensation: 1MHz
Rated at 50V:NPO, X7R, Z5U, Y5V 1Vrms/Fpr high Dielectric constant 1KHz, 1Vrms



Typical X7R, Z5U, Y5V Temperature vs. Capacitance



EIA Standard code for capacitance

The standard capacitance values over 10pF are :

E3 SERIES	E6 SERIES	E12 SERIES	E24 SERIES	
1.0	1.0	1.0	1.0	1.1
		1.2	1.2	1.3
	1.5	1.5	1.5	1.6
		1.8	1.8	2.0
2.2	2.2	2.2	2.2	2.4
		2.7	2.7	3.0
	3.3	3.3	3.3	3.6
		3.9	3.9	4.3
4.7	4.7	4.7	4.7	5.1
		5.6	5.6	6.2
	6.8	6.8	6.8	7.5
		8.2	8.2	9.1

NPO : E12 series (standard)
E24 series (option)
X7R : E6 series (standard)
E12 series (option)
Z5U/Y5V : E3 series (standard)
E6 series (option)

Sorts of dielectric material from which they are made

1) Ceramic
2) Tantalum
3) Electrolytic Aluminum
4) Polymer, OS - Con etc.

Different type of capacitor has characteristics make them suitable for given applications, but not for others.

How a MultiLayer ceramic capacitor is formed

A number of conductive electrodes lay-down(Pd/Ag/Ni/Cu) seperated by an insulation dielectric sheet

Capacitors in Series

1) $C_{total} = \frac{C1+C2+...Cn}{N}$

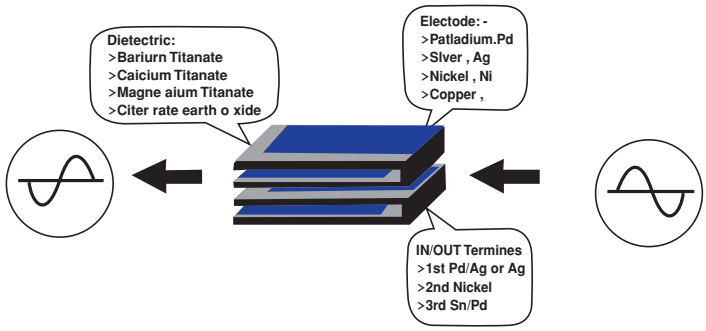
2) Current the same.

Capacitors in Parallel

1) Ctotal=C1+C2+...Cn
2) Voltage the same.

Standard unit of capacitance"F or Farad"

uF=micro Farad=10^{-6}F
nF=nano Farad=10^{-9}F
pF=pico Farad=10^{-12}F



Ceramic Dielectric EIA Definations

Example : A capacitor with X7R code presents the capacitance to be±15% of initial value @ 25℃ from -55 to + 125℃

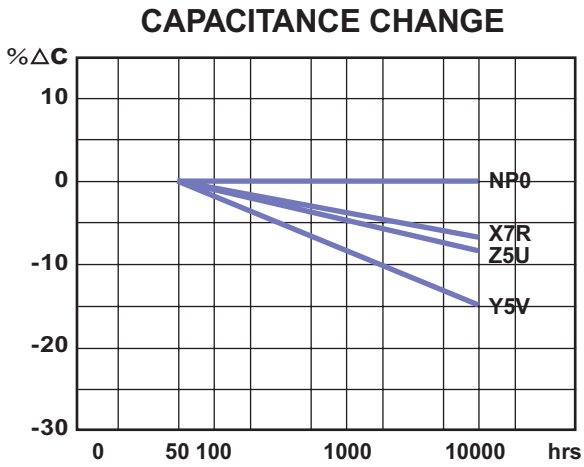
EIA Percentage Capacity Change Over Temperature Range			
RS-198	Temperature Range	Code	Percent Capacity Change or PPM/℃
C0	0	G	±30
		H	±60
X7	-55℃ to +125℃	D	±3.3%
X5	-55℃ to +85℃	E	±4.7%
Y5	-30℃ to +85℃	F	±7.5%
Z5	+10℃ to +85℃	P	±10%
		R	±15%
		T	+22%,-33%
		U	+22%,-56%
		V	+22%,-82%

Voltage and AC

As a general rule, AC must not exceed 10% of the rated DC value, if the AC voltage behaves too powerful on the capacitor, the inner dielectric would heat-up and dissipation becomes an issue, unusual AC spikes or surges can lead to over- heating and the dielectric would rupture or even on fire, This design rule shall be strickly followed, particularly in the application above IKHZ switching frequency.

AGEING PHENOMENON

What is ageing of class Ⅱ caramic (change of capacitance over time)
Ageing is the Shelf-Loss in capacitance that occurs over time and is a normal process of class Ⅱ ceramic capacitors, because of the re-ordering of crystalline structure
When a class Ⅱ ceramic body is cool from its CURIE POINT @ 150℃ and without voltage applied, then the ageing starts under a given ratio designated by vendor



Recovery of ageing – (Deageing)

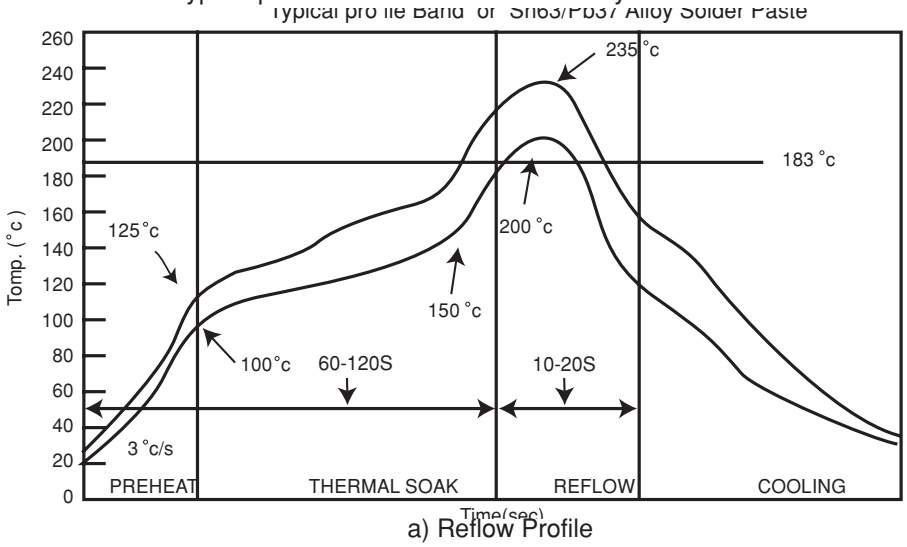
1) Heat - up the device @ 150℃ 1hour or above, the higher temperature the less time required.
2) Voltage slows very much the ageing behaviors of class Ⅱ ceramic capacitors.

Handle guidelines of ageing part

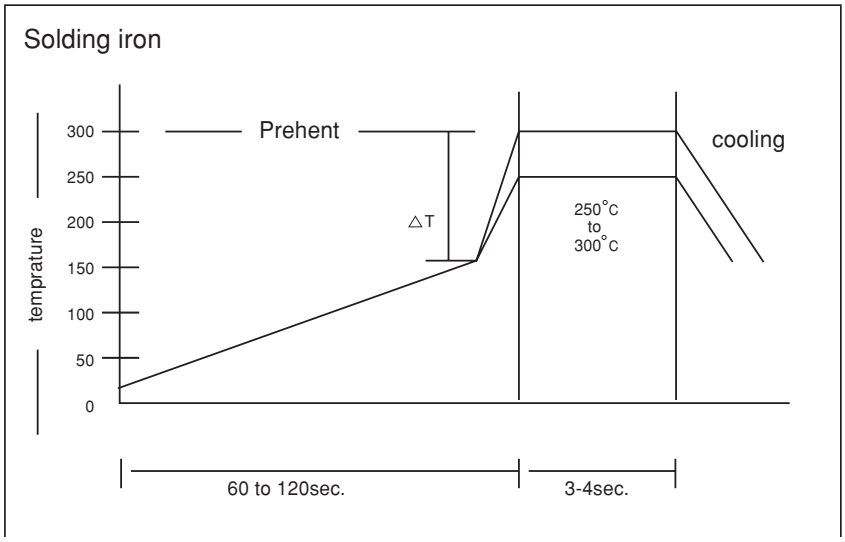
1)The ageing parts will not lead to any reliability issue, but capacitance out from its lower limit which might be observed prior to production...
2)Afer de-ageing process, the parts would back to its initial designated level of capacitance characteristic and another ageing cycle begins when parts putting back to the storage shelf
3)Typically, a process of IR reflow or wave soldering can easily recure the ageing part since it all working at much higher temperature than 150℃ even few seconds dwelling time is far enough for staying at such 210℃~260℃ range.
4)Remeasurement of de-ageing parts, must to wait at least 48 hours @ room temperature.
While the part has cool down, then the capacitance is stable and shall be well within its nominal limit.

Soldering Recommendation

Typical profile Band for sn63/Pb37 Alloy Solder Paste

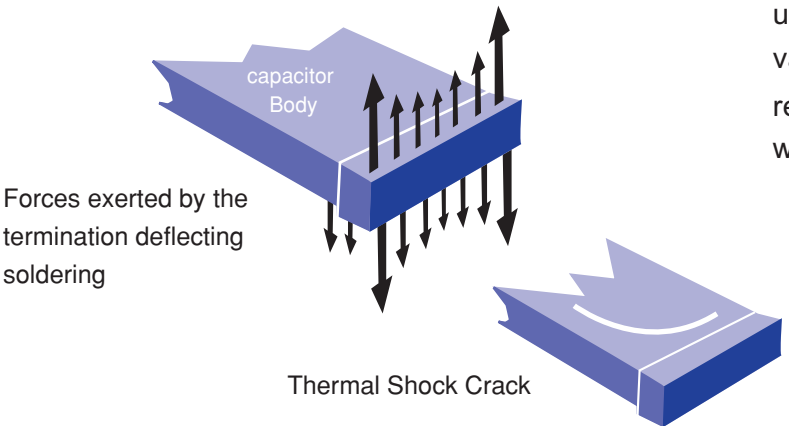


a) Reflow Profile



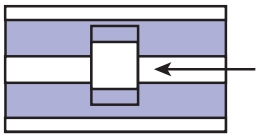
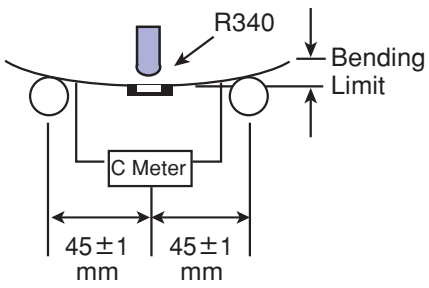
b) Mannal solder iron Profile

Thermal Shock



1)Ceramic is easily damagad from rapid heat-up or cooling due to it's themal expansion of varieties of inner material. it is highly recommended to limit the △ T to within 100℃ when possible.

5. Reliability And Test Conditions

<table>
<tr><th>No</th><th>Test Item</th><th>Specifications</th><th>Test Conditions</th></tr>
<tr><td rowspan="3">1</td><td>Capacitance
Class I
NPO</td><td>Within The Specified Tolerance</td><td>
<table>
<tr><td>Capacitance</td><td>Frequency</td><td>Signal Voltage</td></tr>
<tr><td>C≦1000 pF</td><td>1MHz±10%</td><td>1.0 ± 0.2Vrms</td></tr>
<tr><td>C＞1000 pF</td><td>1KHz±10%</td><td>1.0 ± 0.2Vrms</td></tr>
</table>
</td></tr>
<tr><td>Capacitance
Class II</td><td>Within The Specified Tolerance</td><td>
<table>
<tr><td>Capacitance</td><td>Temp.Char.</td><td>Frequency</td><td>Signal Voltage</td></tr>
<tr><td rowspan="3">C≦22uF</td><td>X7R / X5R</td><td>1KHz ± 10%</td><td>1.0 ± 0.2Vrms</td></tr>
<tr><td>Y5V</td><td>1KHz ± 10%</td><td>1.0 ± 0.2Vrms</td></tr>
<tr><td>Z5U / Y5U</td><td>1KHz ± 10%</td><td>0.5 ± 0.2Vrms</td></tr>
<tr><td colspan="2">C＞22uF</td><td>120HZ± 20%</td><td>0.5± 0.2Vrms</td></tr>
</table>
</td></tr>
<tr><td rowspan="2">2</td><td>Q
Class I
NPO</td><td>C＞30 pF : Q≧1000
C≦30 pF : Q≧400+20×C
(C:Capacitance , pF)</td><td>
<table>
<tr><td>Capacitance</td><td>Frequency</td><td>Signal Voltage</td></tr>
<tr><td>C≦1000 pF</td><td>1MHz±10%</td><td>1.0 ＞0.2Vrms</td></tr>
<tr><td>C＞1000 pF</td><td>1KHz±10%</td><td>1.0 ±0.2Vrms</td></tr>
</table>
</td></tr>
<tr><td>Tan δ
Class II</td><td>
<table>
<tr><td>Temp.Char.</td><td>HI-V</td><td>50V</td><td>25V</td><td>16V</td><td>10V</td><td>6.3V</td></tr>
<tr><td>X7R / X5R</td><td>2.5%</td><td>2.5%</td><td>3.5%</td><td>3.5%</td><td>5%</td><td>5%</td></tr>
<tr><td>Y5V</td><td>5%</td><td>5%</td><td>7%</td><td>9%</td><td>12.5%</td><td>16%</td></tr>
<tr><td>Z5U / Y5U</td><td>4%</td><td>4%</td><td>4%</td><td>4%</td><td>-</td><td>-</td></tr>
</table>
</td><td>
<table>
<tr><td>Temp.Char.</td><td>Frequency</td><td>Signal Voltage</td></tr>
<tr><td>X7R / X5R</td><td>1KHz±10%</td><td>1.0±0.2Vrms</td></tr>
<tr><td>Y5V</td><td>1KHz±10%</td><td>1.0±0.2Vrms</td></tr>
<tr><td>Z5U / Y5U</td><td>1KHz±10%</td><td>0.5±0.2Vrms</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>Insulation
Resistance</td><td>Rated Voltage≧25V 10,000 MΩor 500MΩ÷uF
Rated Voltage≦16V 10,000 MΩor 100MΩ÷uF
Product Whichever Is Smaller</td><td>Vr≦500V Applied Voltage:Rated Voltage
Vr≧500V Applied Voltage:500V
Applied Voltage
Charge Time:60 sec.</td></tr>
<tr><td>4</td><td>Withstanding
Voltage</td><td>No Dielectric Breakdown or Mechanical Breakdown</td><td>Vr＜100V Class I:300% of The Rated Voltage
Class II:250% of The Rated Voltage
Vr=100V 250% of The Rated Voltage
250V≦Vr＜500V 200% of The Rated Voltage
500V≦Vr＜1KV 150% of The Rated Voltage
Vr≧1KV 120% of The Rated Voltage
For 1~5 sec. Is Applied Less Than 50mA Current</td></tr>
<tr><td>5</td><td>Adhesive
Strength
Of
Termination</td><td>No Indication Of Peeling Shall Occur On The Terminal Electrode.</td><td>A 500g..f Push or Pull Force Shall Be Applied For 10±1 Seconds
 
500g.f</td></tr>
<tr><td>6</td><td>Resistance
To
Flexure
Of
Substrate</td><td>No Mechanical Damage Shall Occur.
<table>
<tr><td rowspan="11">C-Meter</td><td>Temp. Char.</td><td>Cap. Change.</td></tr>
<tr><td>NPO</td><td>≦±5 %</td></tr>
<tr><td>X7R</td><td rowspan="2">≦±12.5 %</td></tr>
<tr><td>X5R</td></tr>
<tr><td>Y5V</td><td rowspan="3">≦± 30 %</td></tr>
<tr><td>Y5U</td></tr>
<tr><td>Z5U</td></tr>
<tr><td colspan="2">Chip Array Capacitor</td></tr>
<tr><td>NPO</td><td>≦±1 %</td></tr>
<tr><td>X7R</td><td rowspan="2">≦±10 %</td></tr>
<tr><td>X5V</td></tr>
</table>
</td><td>Bending Shall Be Applied To The 1.0 mm
With 1.0 mm / sec
 
</td></tr>
</table>

<table>
<tr><td rowspan="6">7</td><td rowspan="6">Vibration</td><td colspan="4">No Mechanical Damage Shall Be Occur</td><td rowspan="6"></td></tr>
<tr><td rowspan="4">Capacitance</td><td colspan="2">Temp. Char.</td><td>Cap. Change</td><td rowspan="5">Vibrate The Capacitor With Amplitude Of 1.5mm P-P Changing The Frequencies From 10Hz to 55Hz And Back To 10Hz In About 1 min.</td></tr>
<tr><td>Class I</td><td>NPO</td><td>Within ±2.5%Or±0.25pF Whichever Is Larger</td></tr>
<tr><td rowspan="2">Class II</td><td>X7R / X5R</td><td>Within ±7.5 %</td></tr>
<tr><td>Y5V/Y5U/Z5U</td><td>Within ±20 %</td></tr>
<tr><td>Q
Class I</td><td colspan="3">C＞30pF : Q ≧1000
C≦30pF : Q ≧400＋20×C</td></tr>
<tr><td>Tan δ
Class II</td><td colspan="3">To Satisfy The Specified Initial Value</td></tr>
<tr><td>Insulation Resistance</td><td colspan="3">To Satisfy The Specified Initial Value</td></tr>
<tr><td rowspan="8">8</td><td rowspan="8">Capacitance Temperatrue Coefficient</td><td rowspan="2">Class I</td><td>Temp.Char.</td><td>Temp. Range</td><td>Cap. Change</td><td rowspan="8">Class I:
$\frac{C2-C1}{C1(T2-T1)} \times 100\%$
Class II :
$\frac{C2-C1}{C1} \times 100\%$
T1:Standard Temperatrue (25˚C)
T2:Test Temperature
C1:Capacitance At Standard Temperatrue (25˚C)
C2:Capacitance At Test Temperature (T2)</td></tr>
<tr><td>NPO</td><td>-55˚C~+125˚C</td><td>±30 ppm /˚C</td></tr>
<tr><td rowspan="6">Class II</td><td>Temp.Char.</td><td>Temp. Range</td><td>Cap. Change</td></tr>
<tr><td>X7R</td><td>-55˚C~+125˚C</td><td>±15 %</td></tr>
<tr><td>X5R</td><td>-55˚C~+85˚C</td><td>±15 %</td></tr>
<tr><td>Y5V</td><td>-30˚C~+85˚C</td><td>+ 22 % ~ - 82 %</td></tr>
<tr><td>Y5U</td><td>-30˚C~+85˚C</td><td>+ 22 % ~ - 56 %</td></tr>
<tr><td>Z5U</td><td>+10˚C~+85˚C</td><td>+ 22 % ~ - 56 %</td></tr>
<tr><td>9</td><td>Solderability</td><td colspan="3">More Than 75% of The Terminal Surface Is To Be Soldered Newly, So Metal Part Does Not Come Out Or Dissolve</td><td>Solder Temperature : 230±5 ˚C
Dip Time : 2±0.5 sec.
Solder : H63A
Flux : Rosin
Preheat : At 80~120˚C For 10~30 sec.</td></tr>
<tr><td rowspan="7">10</td><td rowspan="7">Resistance To Soldering Heat</td><td colspan="4">No Mechanical Damage Shall Be Occur</td><td rowspan="7">Class II capacitor shall be set for 48±4 hours at room temperature after one hour heat treatment at 150+0/-10 ˚C before initial measure.
Preheat : At 150±10˚C For 60~120sec.
Dip : Solder Temperatrue of 260±5˚C
Dip Time : 10±1sec.
Solder : H63A
Flux : Rosin

Measure At Room Temp. After Cooling For:
Class I : 24±2 Hours
Class II : 48±4 Hours</td></tr>
<tr><td rowspan="3">Capacitance</td><td colspan="2">Temp. Char.</td><td>Cap. Change</td></tr>
<tr><td>Class I</td><td>NPO</td><td>Within ±2.5%Or±2.5pF Whichever Is Larger</td></tr>
<tr><td rowspan="2">Class II</td><td>X7R / X5R</td><td>Within ±10 %</td></tr>
<tr><td>Y5V/Y5U/Z5U</td><td>Within ±20 %</td></tr>
<tr><td>Q
Class I</td><td colspan="3">C＞30 pF : Q≧1000
C≦30 pF : Q≧400+20×C</td></tr>
<tr><td>Tan δ
Class II</td><td colspan="3">To Satisfy The Specified Initial Value</td></tr>
<tr><td>Insulation Resistance</td><td colspan="3">To Satisfy The Specified Initial Value</td></tr>
<tr><td>Withstand Voltage</td><td colspan="3">To Satisfy The Specified Initial Value</td></tr>
</table>

11 Temperature Cycle

No Mechanical Damage Shall Be Occur

Capacitance	Temp. Char.		Cap. Change
	Class I	NPO	Within ±2.5%Or±2.5pF Whichever Is Larger
	Class II	X7R / X5R	Within ±7.5 %
		Y5V/Y5U/Z5U	Within ± 20 %
Q Class I	C＞30pF : Q ≧1000 C≦30pF : Q ≧400＋20×C		

Tan δ Class II	Temp. Char.	HI-V	50V	25V	16V	10V	6.3V
	X7R / X5R	2.5%	2.5%	3.5%	3.5%	5%	5%
	Y5V	5%	5%	7%	9%	12.5%	16%
	Y5U / Z5U	4%	4%	4%	4%	-	-

Insulation Resistance: To Satisfy The Specified Initial Value

Class II capacitor shall be set for 48±4 hours at room temperature after one hour heat treatment at 150+0/-10 ˚C before initial measure.
Capacitor Shall Be Subjected To Five Cycles Of The Temperature Cycle As Following:

Step	Temp (˚C)	Time(min)
1	Min Rated Temp +0/-3	30
2	25	3
3	Max Rated Temp +0/-3	30
4	25	3

Measure At Room Temp. After Cooling For:
Class I : 24 ±2 Hours
Class II : 48 ±4 Hours

12 High Temperature

No Mechanical Damage Shall Be Occur

Capacitance	Temp. Char.		Cap. Change
	Class I	NPO	Within ±3.0% Or ±0.3pF Whichever Is Larger
	Class II	X7R / X5R	Within ±15 %
		Y5V/Y5U/Z5U	Within ±30 %
Q Class I	C＞30pF : Q ≧350 10 pF＜C≦30 pF : Q ≧275＋2.5×C C≦10 pF : Q ≧200＋10×C		

Tan δ Class II	Temp. Char.	HI-V	50V	25V	16V	10V	6.3V
	X7R / X5R	5%	5%	7%	7%	10%	10%
	Y5V	7.5%	7.5%	10.5%	12.5%	15%	16%
	Y5U / Z5U	5%	6%	10.5%	10.5%	-	-

Class II capacitors applied DC voltage of 120% the rated voltage is applied for one hour at maximum operation temperature ±3˚C then shall be set for 48 ± 4 hours at room temperature and the initial measurement shall be conducted.
Applied Voltage : 120% Of Rated Voltage
Temperature :Maximum Operation Temperature
Test Time : 1000 ＋48/−0 Hour
Current Applied : 50mA Max.
Measurement Room Temperature
After Cooling For :
Class¢π : 24 ± 2 Hours
Class¢∫ : 48 ± 4 Hours

13 Humidity

No Mechanical Damage Shall Be Occur

Capacitance	Temp. Char.		Cap. Change
	Class I	(NPO)	Within±5%Or±5pF Whichever Is Larger
	Class II	X7R / X5R	Within ±15 %
		Y5V/Y5U/Z5U	Within ± 30 %
Q Class I	C＞30pF : Q ≧350 10 pF＜C≦30 pF : Q ≧275＋2.5×C C≦10 pF : Q ≧200＋10×C		

Tan δ Class II	Temp. Char.	HI-V	50V	25V	16V	10V	6.3V
	X7R / X5R	2.5%	5%	7%	7%	10%	10%
	Y5V	7.5%	7.5%	10.5%	12.5%	15%	16%
	Y5U / Z5U	5%	6%	6%	6%	-	-

Insulation Resistance: Minimum Insulation Resistance : 1000 MΩ or 50 MΩ ÷ μF product whichever is smaller

Class II capacitor shall be set for 48 ±4 hours at room temperature after one hour heat treatment at 150+0/-10 ˚C before initial measure.

Temperature : 40 ±2 ˚C
Relative Humidity : 90 ~ 95 % RH
Test Time : 500+12/-0 Hour
Current Applied : 50mA Max.
Measurement Room Temperature
After Cooling For:
Class I : 24 ± 2 Hours
Class II : 48 ± 4 Hours

<table>
<tr><td rowspan="8">14</td><td rowspan="8">Humidity Load</td><td colspan="8">No Mechanical Damage Shall Be Occur</td><td rowspan="8">Class II capacitors applied DC voltage of the rated voltage is applied for one hour at maximum operation temperature ±3˚C then shall be set for 48 ± 4 hours at room temperature and the initial measurement shall be conducted.
Applied Voltage : Rated Voltage
Temperature : 40 ± 2˚C
Relative Humidity : 90 ~ 95% RH
Test Time : 500＋12/–0 Hour
Current Applied : 50mA Max.
Measurement Room Temperature
After Cooling For :
Class I: 24 ± 2 Hours
Class II: 48 ± 4Hours</td></tr>
<tr><td rowspan="3">Capacitance</td><td colspan="3">Temp. Char.</td><td colspan="4">Cap. Change.</td></tr>
<tr><td colspan="2">Class I</td><td>NPO</td><td colspan="4">Within±7.5%Or
±7.5pF
Whichever Is Larger</td></tr>
<tr><td colspan="2">Class II</td><td>X7R / X5R
Y5V/Y5U/Z5U</td><td colspan="4">Within ±12.5 %
Within ± 30 %</td></tr>
<tr><td rowspan="2">Q
Class I</td><td colspan="7">C＞30pF : Q ≧350
10 pF＜C≦30 pF : Q ≧275＋2.5×C
C≦10 pF : Q ≧200＋10×C</td></tr>
<tr><td colspan="7">Chip Array Capaitor
C＞30pF : Q ≧200
C≦30 pF : Q ≧200＋10/3×C</td></tr>
<tr><td rowspan="4">Tan δ
Class II</td><td>Temp. Char.</td><td>HI-V</td><td>50V</td><td>25V</td><td>16V</td><td>10V</td><td>6.3V</td></tr>
<tr><td>X7R / X5R</td><td>2.5%</td><td>5%</td><td>7%</td><td>7%</td><td>10%</td><td>10%</td></tr>
<tr><td>Y5V</td><td>7.5%</td><td>7.5%</td><td>10.5%</td><td>12.5%</td><td>15%</td><td>16%</td></tr>
<tr><td>Y5U / Z5U</td><td>5%</td><td>6%</td><td>6%</td><td>6%</td><td>-</td><td>-</td></tr>
<tr><td>Insulation Resistance</td><td colspan="7">Minimum Insulation Resistance :
500 MΩ or 25MΩ ÷ μF
product whichever is smaller</td></tr>
</table>

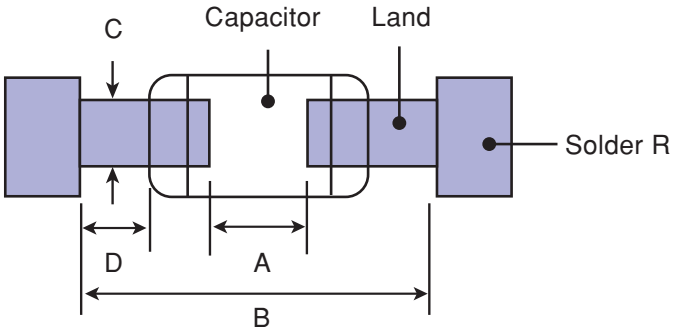
1. Storage

Store the capacitors where the temperature and relative humidity don't exceed 40℃ and 70%RH. We recommend you use capacitors within 6 months from the manufactured date. In case of packaging, don't the last wrapped, polyethylene bag, till just before using. If it is opened, seal it as soon as possible or keep it in a desiccant with a desiccantion agent.

2.Construction of Board Pattern

After installing chips, If solder is excessively applied to the circuit board, mechanical strength will cause destruction resistance characteristic to lower. To prevent this be extremely careful in shape and dimension before designing the circuit board diagram.

2.1 Size and recommend land dimensions.



REFLOW SOLDERING

Code	Chip (mm)		Land (mm)			
	L	W	A	B	C	D
0201	0.60	0.30	0.2 ~ 0.3	0.9 ~ 1.1	0.2 ~ 0.3	0.1 ~ 0.3
0402	1.00	0.50	0.3 ~ 0.5	1.3 ~ 1.5	0.3 ~ 0.5	0.1 ~ 0.3
0603	1.60	0.80	0.6 ~ 0.8	1.9 ~ 2.1	0.6 ~ 0.8	0.2 ~ 0.5
0805	2.00	1.25	0.8 ~ 1.2	2.4 ~ 3.2	0.9 ~ 1.2	0.2 ~ 0.6
1206	3.20	1.60	1.8 ~ 2.5	3.8 ~ 4.8	1.2 ~ 1.6	0.3 ~ 0.8
1210	3.20	2.50	1.9 ~ 2.6	3.9 ~ 4.9	1.9 ~ 2.5	0.3 ~ 0.8
1808	4.50	2.00	2.4 ~ 3.4	5.4 ~ 6.0	1.7 ~ 2.0	0.5 ~ 1.3
1812	4.50	3.20	2.5 ~ 3.5	5.5 ~ 6.1	2.3 ~ 3.2	0.5 ~ 1.3
2220	5.70	5.00	2.7 ~ 4.2	6.7 ~ 8.3	3.5 ~ 5.0	0.5 ~ 1.3

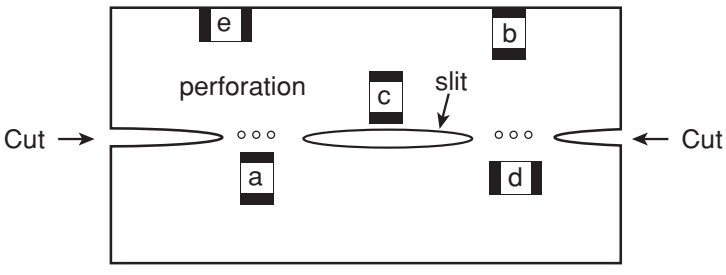
2.2.Mechanical strength varies according to location of chip capacitors the P.C. board.

Design layout of components on the PC board to minimize the stress imposed on the wrap or flexure of the board.

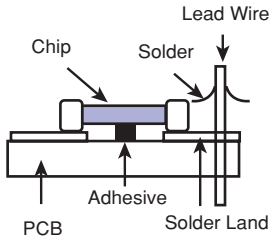
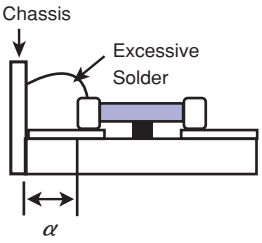
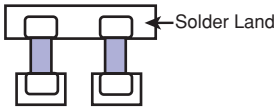
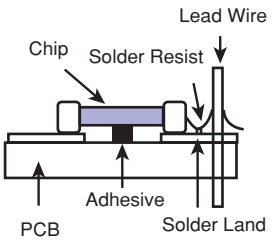
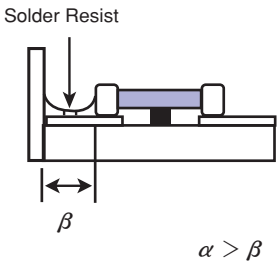
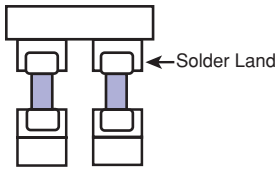
Component layout close to board break

Susceptibility to stress is in the order of :

a>b>c≒d>e



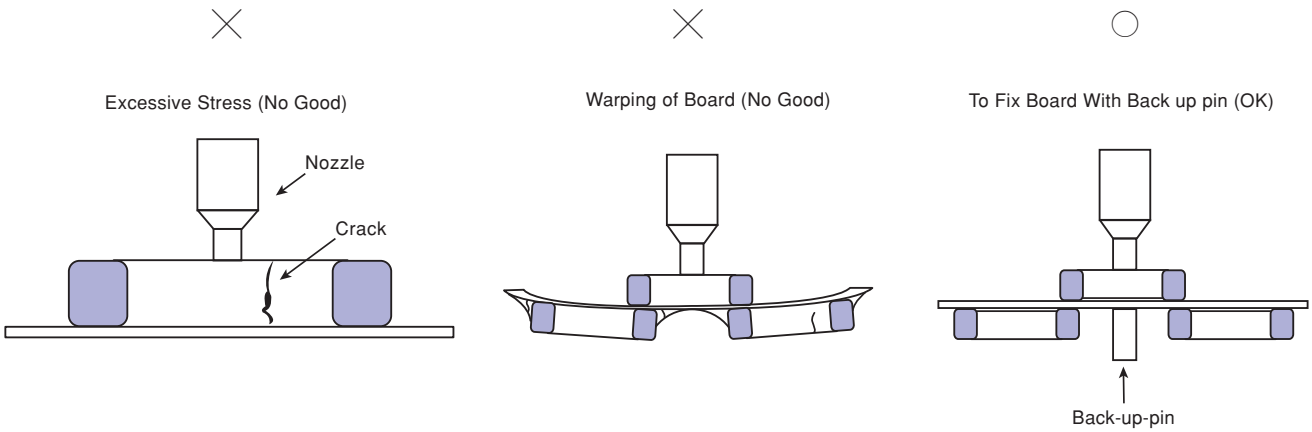
2. 3Layout Recommendation

Example	Use of Common Solder Land	Solder With Chassis	Use of Common Solder Land With Other SMD
Need to Avoid			
Recommendation			

3.Mounting

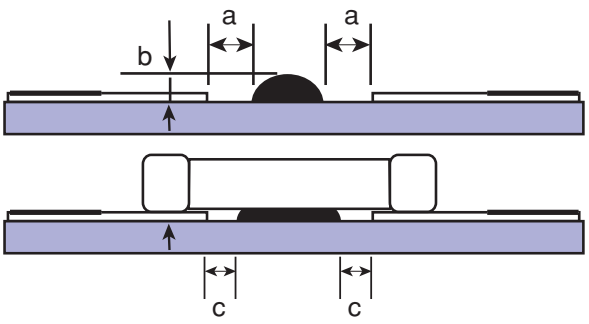
Crack is caused by impact load due to suction nozzle at the mounted.

In mounting an element to board, If the low dead point is too low , excessive stress is applied to element. This will cause cracking. In this case, it is required to shift the low dead point of a suction nozzle to the upper surface of board so that warping of board is eliminated. Nozzle pressure is adjusted to 1N to 3N(static load)during mounting.



If board is warped during mounting, crack or peeling of soldering will be caused. To avoid this, it is required to fix the board with back up pins or the like to avoid warping. Also, similar precautions are required when inserting a part with lead.

4.Amount of Adhesive

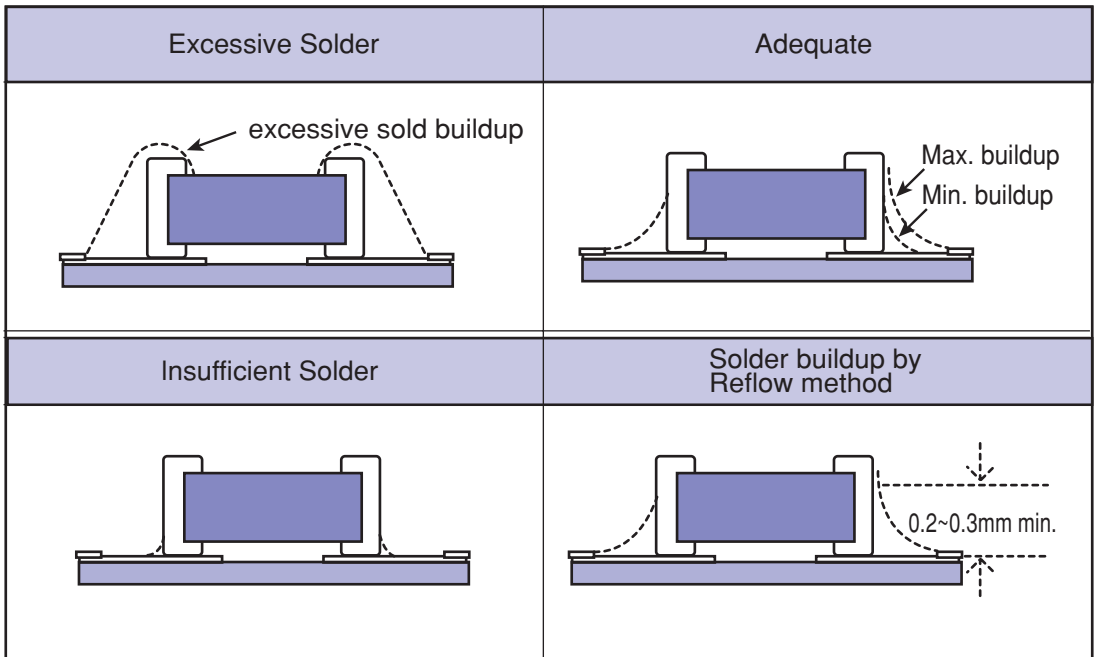


Example: 0805 & 1206

a	0.2mm min
b	70~100 μ m
c	Do not touch the solder land

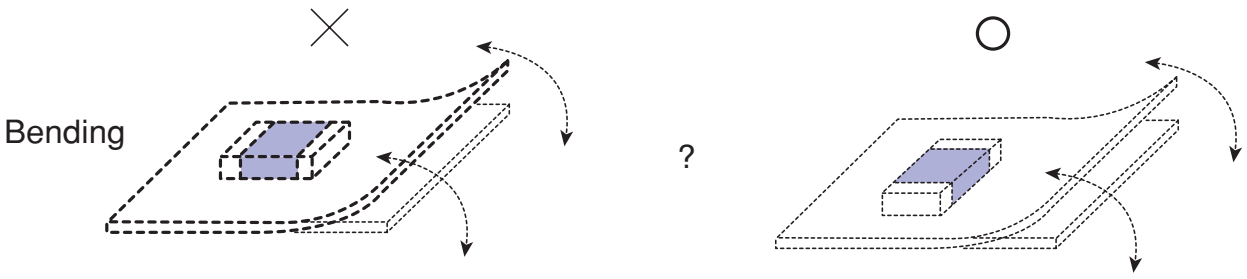
5.Amout of Solder

Excessive solder will induce higher tensile force in chip capacitor when temperature change and it may result in chip cracking. In Sufficient solder may detach the capacitor from the P.C. board.

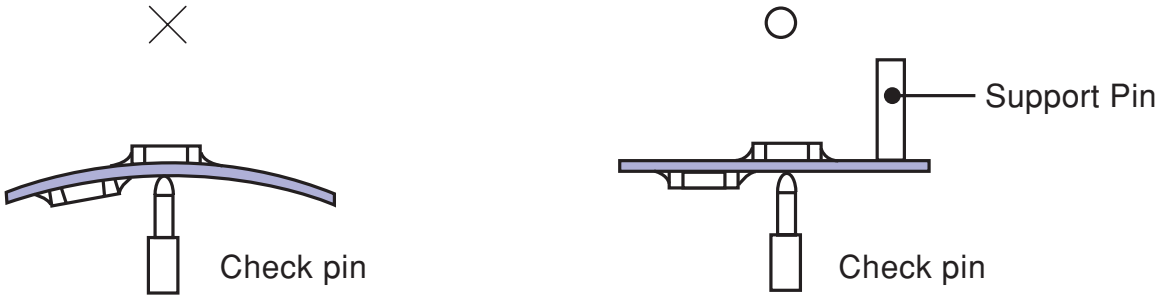


6.Handing after chip mounted

6.1.Please pay attention put the component lateral to the direction in which stress acts.



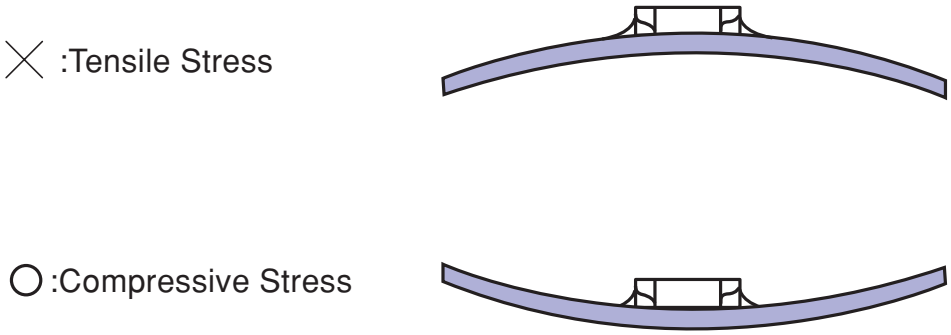
6.2.Crack Will be caused if board is warped due to excessive load by check pin.



6.3Mechanical stress due to warping and torsion by dividing.

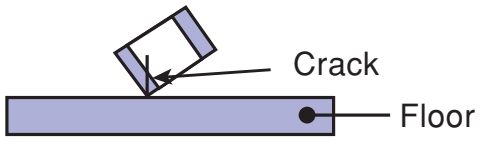
(a) Crack occurrence ratio will be increased by manual separation.

(b) Crack occurrence ratio will be increased by tensile force, rather than compressive force.

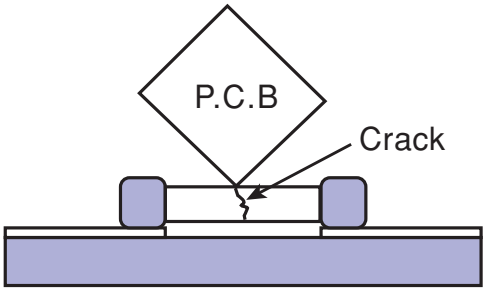


7.Handing to Loose Chip Capacitor

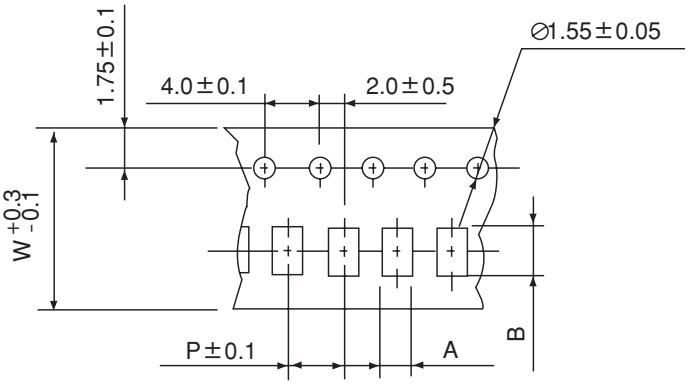
7.1If dropped the chip capacitor may crack.

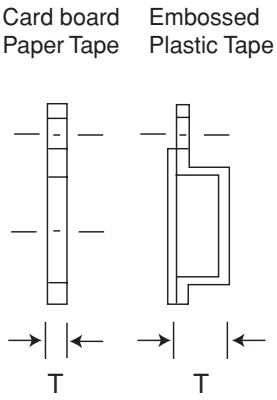


7.2Piling the P.C.board after mounting for storage or handling, the comer of the P.C. board may hit the chip capacitor of another of board to cause crack.



TAPE DIMENSIONS AND PACKAGING QUANTITIES



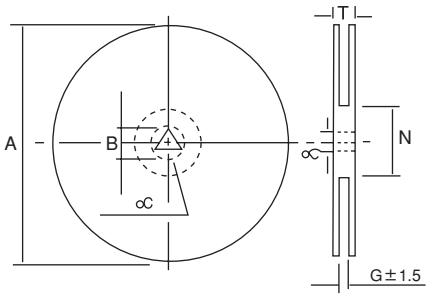


Unit : mm

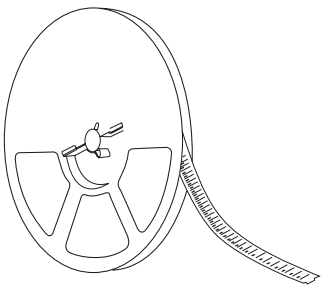
Type	A	B	W	P	T	(pcs)/Reel
0201	0.37±0.05	0.67±0.05	8	2	1.2 max	15K
0402	0.65±0.1	1.15±0.1	8	2	1.2 max	10K
0603	1.1±0.2	1.9±0.2	8	4	1.2 max	4K
0805	1.5±0.2	2.3±0.2	8	4	2.5 max	4K/3K/2K
1206	1.9±0.2	3.5±0.2	8	4	2.5 max	4K/3K
1210	2.9±0.2	3.6±0.2	8	4	3.8 max	3K/2K/1K
1808	2.5±0.3	4.9±0.3	8	4	3.8 max	3K/2K/1K
1812	3.6±0.3	4.9±0.3	8	4	3.8 max	1K/500
2220	5.4±0.3	6.1±0.3	8	4	3.8 max	1K/500

REEL DIMENSIONS

Material:Paper,Plastic



Reel Packaging



Unit : mm

Type	8 mm	12 mm
A	178+2	178+2
B	21+0.8	21+0.8
C	13+0.8	13+0.8
G	10	14
N	75	75
T	12.5	16.5