PIC18F1XK22/LF1XK22
Data Sheet

20-Pin Flash Microcontrollers with nanoWatt XLP Technology

PIC18F1XK22/LF1XK22

20-Pin Flash Microcontrollers with nanoWatt XLP Technology

High-Performance RISC CPU:

- C Compiler Optimized Architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 256 bytes Data EEPROM
- Up to 16 Kbytes Linear Program Memory Addressing
- Up to 512 bytes Linear Data Memory Addressing
- Up to 16 MIPS Operation
- 16-bit Wide Instructions, 8-bit Wide Data Path
- Priority Levels for Interrupts
- 31-Level, Software Accessible Hardware Stack
- 8 x 8 Single-Cycle Hardware Multiplier

Flexible Oscillator Structure:

- Precision 16 MHz Internal Oscillator Block:
  - Factory calibrated to ± 1%
  - Software selectable frequencies range of 31 kHz to 16 MHz
  - 64 MHz performance available using PLL – no external components required
- Four Crystal modes up to 64 MHz
- Two External Clock modes up to 64 MHz
- 4X Phase Lock Loop (PLL)
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if peripheral clock stops
- Two-Speed Oscillator Start-up

Special Microcontroller Features:

- Full 5.5V Operation – PIC18F1XK22
- 1.8V-3.6V Operation – PIC18LF1XK22
- Self-reprogrammable under Software Control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Brown-out Reset (BOR)
- Extended Watchdog Timer (WDT):
  - Programmable period from 4ms to 131s
- Programmable Code Protection
- In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug via Two Pins

Extreme Low-Power Management PIC18LF1XK22 with nanoWatt XLP:

- Sleep mode: 34 nA
- Watchdog Timer: 460 nA
- Timer1 Oscillator: 650 nA @ 32 kHz

Analog Features:

- Analog-to-Digital Converter (ADC) module
  - 10-bit resolution, 12 channels
  - Auto acquisition capability
  - Conversion available during Sleep
- Analog Comparator module:
  - Two rail-to-rail analog comparators
  - Independent input multiplexing
  - Inputs and outputs externally accessible
- Voltage Reference module:
  - Programmable (% of V_{DD}), 16 steps
  - Two 16-level voltage ranges using V_{REF} pins
  - Programmable Fixed Voltage Reference (FVR), 3 levels

Peripheral Highlights:

- 17 I/O Pins and 1 Input-only Pin:
  - High current sink/source 25 mA/25 mA
  - Programmable weak pull-ups
  - Programmable interrupt-on- change
  - Three external interrupt pins
- Four Timer modules:
  - 3 16-bit timers/counters with prescaler
  - 1 8-bit timer/counter with 8-bit period register, prescaler and postscaler
  - Dedicated, low-power Timer1 oscillator
- Enhanced Capture/Compare/PWM (ECCP) module:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and Auto-restart
  - PWM output steering control
- Master Synchronous Serial Port (MSSP) module
  - 3-wire SPI (supports all 4 SPI modes)
  - I^2C™ Master and Slave modes (Slave mode address masking)
- Enhanced Universal Synchronous Asynchronous Receiver Transmitter module (EUSART)
  - Supports RS-232, RS-485 and LIN 2.0
  - Auto-Baud Detect
  - Auto Wake-up on Break
- SR Latch (555 Timer) module with:
  - Configurable inputs and outputs
  - Supports mTouch™ capacitive sensing applications

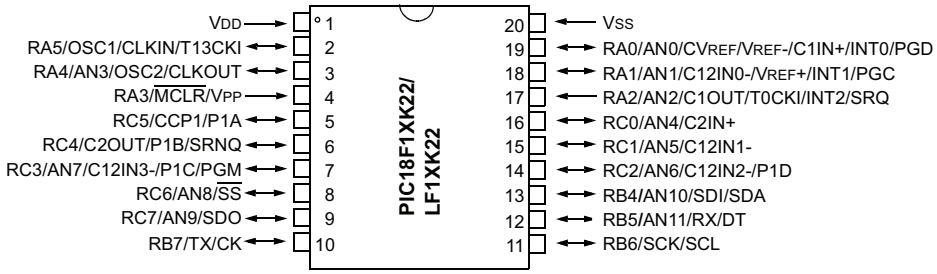
TABLE 1: DEVICE OVERVIEW

Device	Program Memory		Data Memory		Pins	I/O[1]	10-bit A/D Channels	Comparators	Timers 8-bit/16-bit	ECCP	MSSP	EUSART	SR Latch
	Bytes	Words	SRAM (bytes)	Data EEPROM (bytes)									
PIC18F13K22 PIC18LF13K22	8K	4K	256	256	20	18	12-ch	2	1 / 3	1	1	1	Yes
PIC18F14K22 PIC18LF14K22	16K	8K	512	256	20	18	12-ch	2	1 / 3	1	1	1	Yes

Note 1: One pin is input-only.

Pin Diagrams

20-pin PDIP, SSOP, SOIC (300 MIL)



20-Pin QFN 4x4

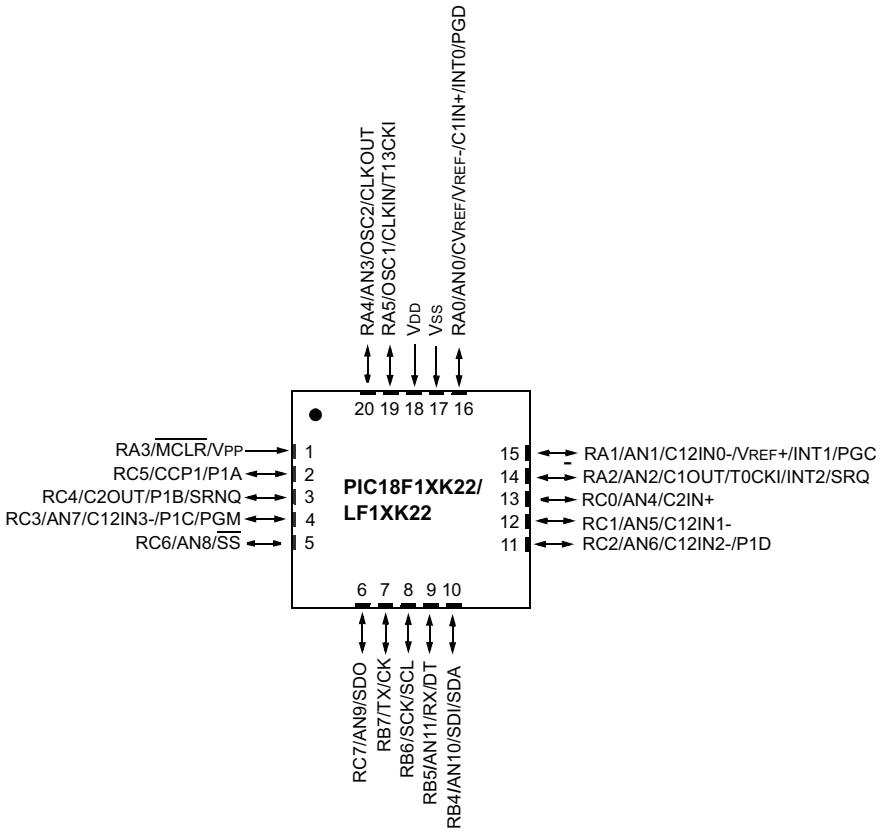


TABLE 1-1: PIC18F1XK22/LF1XK22 PIN SUMMARY

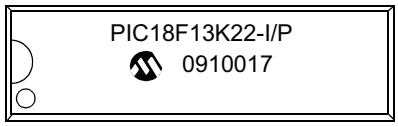
20-Pin DIL	20-Pin QFN	I/O	Analog	Comparator	Reference	ECCP	EUSART	MSSP	SR Latch	Timers	Interrupts	Pull-up	Basic
19	16	RA0	AN0	C1IN+	VREF-/CVREF	—	—	—	—	—	IOC/INT0	Y	PGD
18	15	RA1	AN1	C12IN0-	VREF+	—	—	—	—	—	IOC/INT1	Y	PGC
17	14	RA2	AN2	C1OUT	—	—	—	—	SRQ	T0CKI	IOC/INT2	Y	—
4	1	RA3	—	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$/VPP
3	20	RA4	AN3	—	—	—	—	—	—	—	IOC	Y	OSC2/CLKOUT
2	19	RA5	—	—	—	—	—	—	—	T13CKI	IOC	Y	OSC1/CLKIN
13	10	RB4	AN10	—	—	—	—	SDI/SDA	—	—	IOC	Y	—
12	9	RB5	AN11	—	—	—	RX/DT	—	—	—	IOC	Y	—
11	8	RB6	—	—	—	—	—	SCL/SCK	—	—	IOC	Y	—
10	7	RB7	—	—	—	—	TX/CK	—	—	—	IOC	Y	—
16	13	RC0	AN4	C2IN+	—	—	—	—	—	—	—	—	—
15	12	RC1	AN5	C12IN1-	—	—	—	—	—	—	—		—
14	11	RC2	AN6	C12IN2-	—	P1D	—	—	—	—	—		—
7	4	RC3	AN7	C12IN3-	—	P1C	—	—	—	—	—	—	PGM
6	3	RC4		C2OUT	—	P1B	—	—	SRNQ	—	—	—	—
5	2	RC5	—	—	—	CCP1/P1A	—	—	—	—	—	—	—
8	5	RC6	AN8	—	—	—	—	$\overline{SS}$	—	—	—	—	—
9	6	RC7	AN9	—	—	—	—	SDO	—	—	—	—	—
1	18	—	—	—	—	—	—	—	—	—	—	—	VDD
20	17	—	—	—	—	—	—	—	—	—	—	—	VSS

27.0 PACKAGING INFORMATION

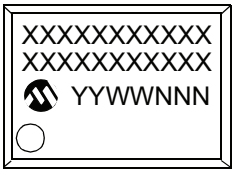
27.1 Package Marking Information

20-Lead PDIP

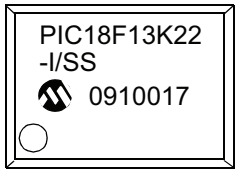
Example



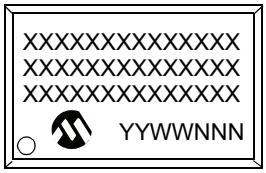
20-Lead SSOP



Example

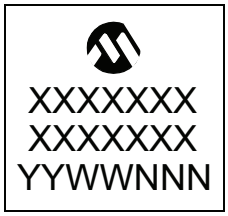


20-Lead SOIC (.300”)



Example

20-Lead QFN



Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

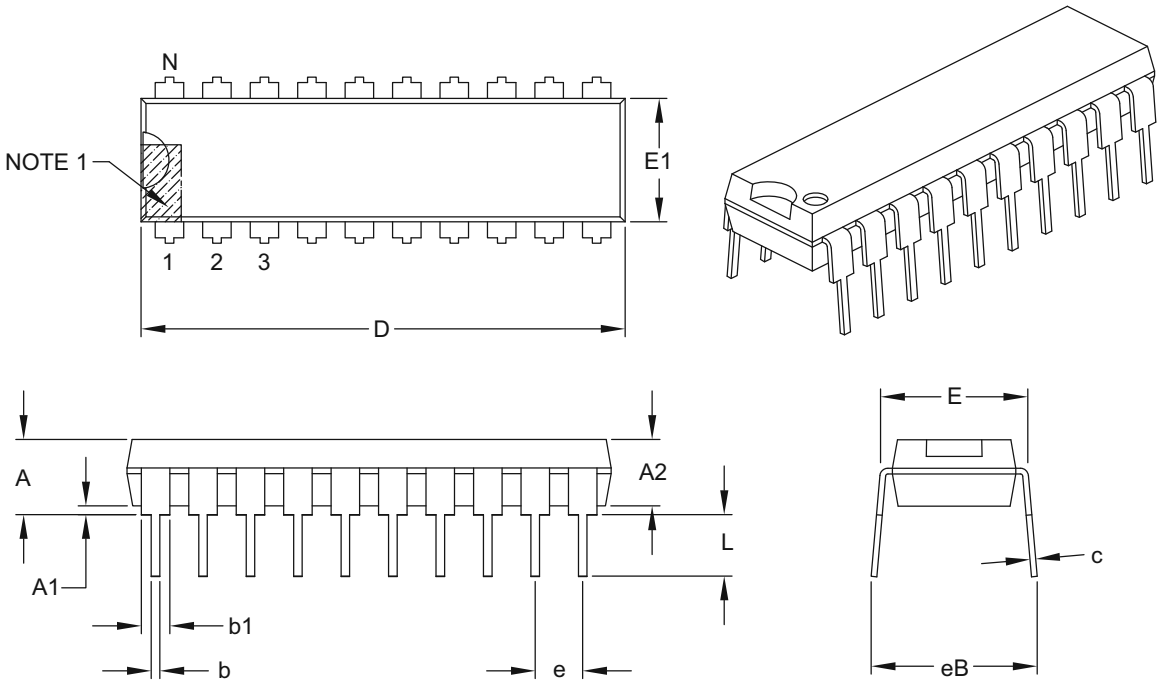
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

27.2 Package Details

The following sections give the technical details of the packages.

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

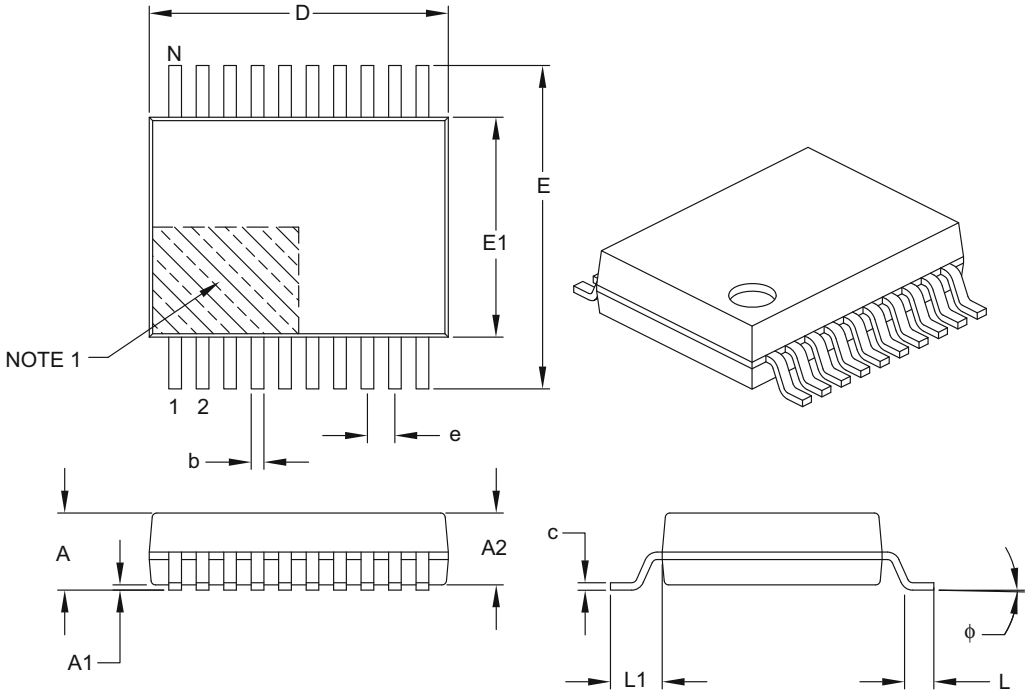
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

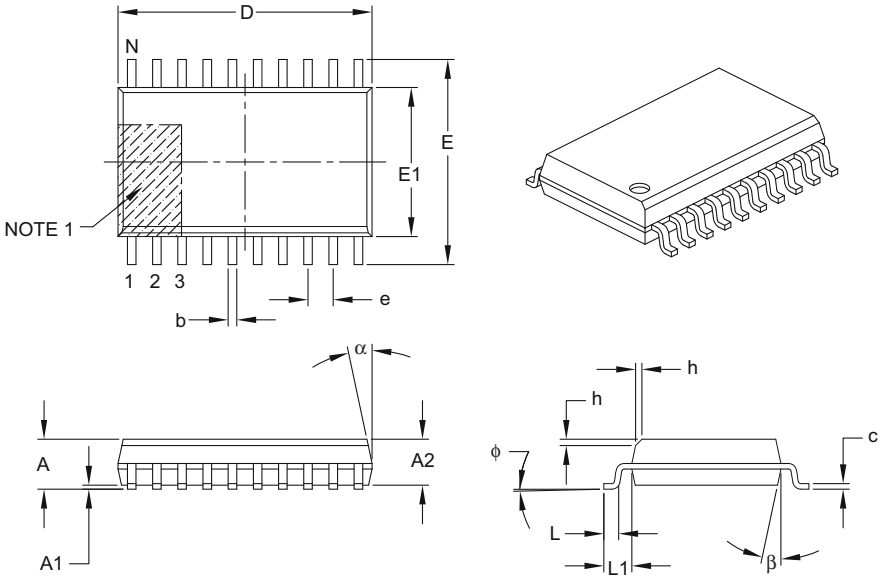
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		12.80 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

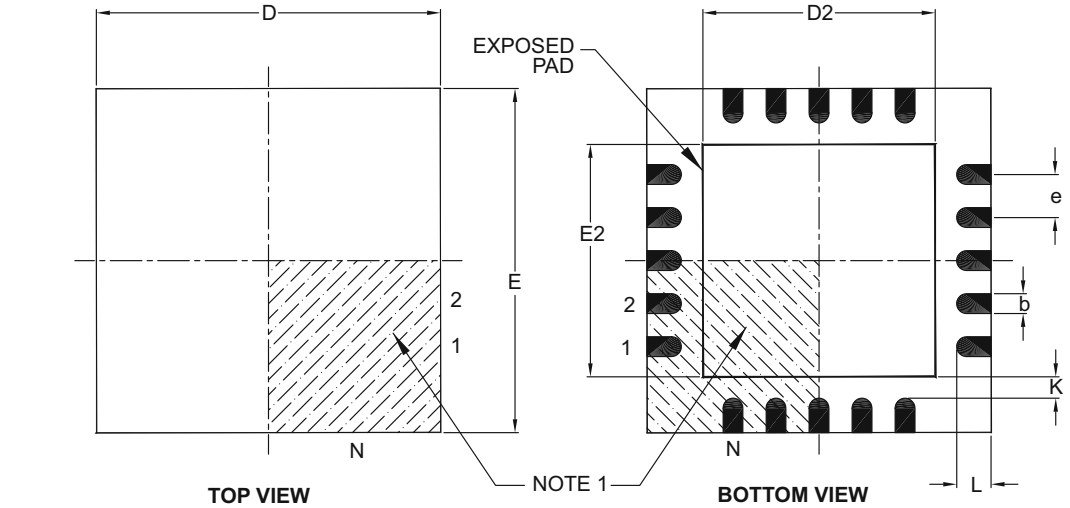
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

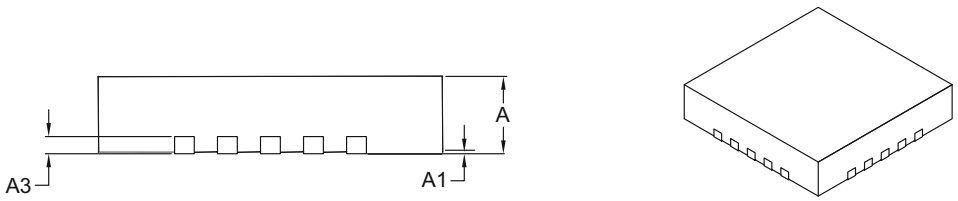
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-094B

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.60	2.70	2.80
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

APPENDIX A: REVISION HISTORY

Revision A (February 2009)

Original data sheet for PIC18F1XK22/LF1XK22 devices.

Revision B (04/2009)

Revised data sheet title; Revised Peripheral Features section; Revised Table 3-1, Table 3-2; Revised Example 15-1; Revised Table 21-4.

Revision C (10/2009)

Updated the Electrical Specifications section (subsections 25.2, 25.3, 25.4, 25.5, 25.6, 25.7, 25.8).

Revision D (05/2010)

Revised Section 1.3 (deleted #2); Revised Figure 1-1; Added Table 2-4; Removed register EEADRH from Tables 3-1 and 3-2; Revised Section 5 (Data EEPROM Memory); Updated Example 5-2 and Table 5-1; Revised Section 13.4.4 (Enhanced PWM Auto-Shutdown Mode); Added Note 4 below Register 13-2; Revised Figure 16-1; Revised Equation 20-1; Removed sub-section 20.1.3 (Output Clamped to VSS); Updated Figure 20-1; Revised Tables 21-4 and Table 22-1; Updated Register 22-5, Figure 25-5, Table 25-2, Table 25-8, Table 25-10 and Table 25-12; Updated the Electrical Specification section; Other minor corrections.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F13K22	PIC18F14K22	PIC18LF13K22	PIC18LF14K22
Program Memory (Bytes)	8192	16384	32768	8192
Program Memory (Instructions)	4096	8192	16384	4096
VDD Max(V)	5.5	5.5	3.6	3.6
Interrupt Sources	19	19	19	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E
Capture/Compare/PWM Modules	1	1	1	1
Enhanced Capture/Compare/PWM Modules	1	1	1	1
Parallel Communications (PSP)	No	No	No	Yes
10-bit Analog-to-Digital Module	11 input channels	11 input channels	11 input channels	14 input channels
Packages	20-pin PDIP 20-pin SOIC 20-pin SSOP 20-Pin QFN	20-pin PDIP 20-pin SOIC 20-pin SSOP 20-Pin QFN	20-pin PDIP 20-pin SOIC 20-pin SSOP 20-Pin QFN	20-pin PDIP 20-pin SOIC 20-pin SSOP 20-Pin QFN

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC18F13K22(1), PIC18F14K22(1), PIC18LF13K22(1), PIC18LF14K22	
Temperature Range:	E = -40°C to +125°C I = -40°C to +85°C	(Extended) (Industrial)
Package:	ML = QFN P = PDIP SO = SOIC SS = SSOP	
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC18F14K22-E/P 301 = Extended temp., PDIP package, Extended VDD limits, QTP pattern #301.

b) PIC18LF14K22-E/SO = Extended temp., SOIC package.

c) PIC18LF14K22-E/P = Extended temp., PDIP package.

Note 1: T = in tape and reel PLCC, and TQFP packages only.