

# SKYPER 42 LJ PV



## Driver Core

Order Number  
L5073102

Datasheet valid for L5073102 Index 01

## SKYPER 42 LJ PV

### Features\*

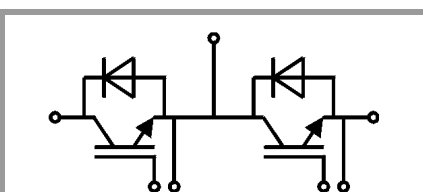
- Two output channels
- Integrated power supply
- Separated failure/signal transmission
- Selectable dead time
- Dynamic short-circuit detection
- SoftOff in case of secondary side error
- Active clamping
- Selectable filter setting
- Multi failure management
- ROHS recognized
- UL approval in progress
- Coated with SL1307

### Typical Applications

- Driver for IGBT modules in bridge circuits in industrial application

### Remarks

- The maximum DC-Link voltage is limited by the creepage and clearance distances; according to EN61800-5-1, PD II, OVC III & EN62109-1, PD II, OVC III
- Operating temperature is real ambient temperature around the driver core
- Environmental conditions see Technical Explanation



Two channel driver core

Absolute Maximum Ratings			
Symbol	Conditions	Values	Unit
$V_s$	Supply voltage primary side	15.6	V
$V_{IH}$	Input signal voltage (HIGH)	$V_s + 0.3$	V
$V_{IL}$	Input signal voltage (LOW)	$GND - 0.3$	V
$I_{out(peak)}$	Output peak current <sup>1)</sup>	35	A
$I_{out(avg)}$	Output average current <sup>1)</sup>	180	mA
$f_{max}$	Maximum switching frequency <sup>2)</sup>	100	kHz
$V_{CE}$	Collector emitter voltage <sup>3)</sup>	1700	V
$V_{DC}$	DC-Link voltage <sup>4)</sup>	1500	V
dv/dt	Rate of rise and fall of voltage secondary to primary side	100	kV/ $\mu$ s
$V_{isol}$	Insulation test voltage <sup>5)</sup>	5000	V
$Q_{out}$	Output charge per pulse <sup>6)</sup>	20	$\mu$ C
$T_{op}$	Operating temperature range	-40 ... 105	$^{\circ}$ C
$T_{stg}$	Storage temperature range	-40 ... 85	$^{\circ}$ C

Characteristics					
Symbol	Conditions	min.	typ.	max.	Unit
$V_s$	Supply voltage primary side	14.4	15	15.6	V
$V_{UVLO(prim)}$	Undervoltage lockout primary side	12.2		13.9	V
$V_{UVLO(secP)}$	Undervoltage lockout secondary side, positive voltage	9.4		13.3	V
$V_{UVLO(secN)}$	Undervoltage lockout secondary side, negative voltage	-5.8		-4.1	V
$I_{S(idle)}$	Supply current primary side (no load)		65		mA
$I_{S(max)}$	Supply current primary side (full load)			990	mA
$V_I$	Input signal voltage on/off		$V_s/0$		V
$V_{IT+}$	Input threshold voltage (HIGH)			8.6	V
$V_{IT-}$	Input threshold voltage (LOW)	6.7			V
$R_{IN(sw)}$	Input resistance (switching signals)		33		k $\Omega$
$C_{IN(sw)}$	Input capacitance (switching signals)			0.01	nF
$V_{G(on)}$	Turn-on output voltage		15.4		V
$V_{G(off)}$	Turn-off output voltage		-8		V
$t_{d(on,ana)}$	Turn-on propagation delay time for analog filter selection		0.5		$\mu$ s
$t_{d(on,dig)}$	Turn-on propagation delay time for digital filter selection		0.83		$\mu$ s
$t_{d(off,ana)}$	Turn-off propagation delay time for analog filter selection		0.5		$\mu$ s
$t_{d(off,dig)}$	Turn-off propagation delay time for digital filter selection		0.83		$\mu$ s
$R_{IN(err,prim)}$	Input resistance (error input, primary side)		150		k $\Omega$
$C_{IN(err,prim)}$	Input capacitance (error input, primary side)		10		nF
$R_{IN(err,sec)}$	Input resistance (error inputs, secondary side)		150		k $\Omega$
$C_{IN(err,sec)}$	Input capacitance (error inputs, secondary side)			0.01	nF
$t_{d(err)}$	Error propagation delay time <sup>7)</sup>		0.7		$\mu$ s
$t_{d(err,ext)}$	External error propagation delay time <sup>8)</sup>		0.6		$\mu$ s
$t_{IDT}$	Interlock dead time <sup>9)</sup>		2		$\mu$ s
$t_{jitter(ana)}$	Signal transfer deviation for analog filter selection <sup>10)</sup>		$\pm 3$		ns

# SKYPER 42 LJ PV



## Driver Core

Order Number  
L5073102

Datasheet valid for L5073102 Index 01

## SKYPER 42 LJ PV

### Features\*

- Two output channels
- Integrated power supply
- Separated failure/signal transmission
- Selectable dead time
- Dynamic short-circuit detection
- SoftOff in case of secondary side error
- Active clamping
- Selectable filter setting
- Multi failure management
- ROHS recognized
- UL approval in progress
- Coated with SL1307

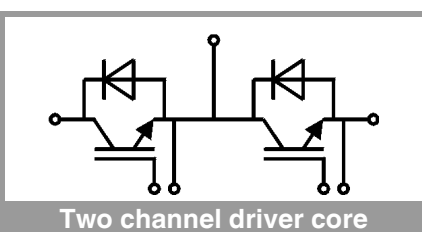
### Typical Applications

- Driver for IGBT modules in bridge circuits in industrial application

### Remarks

- The maximum DC-Link voltage is limited by the creepage and clearance distances; according to EN61800-5-1, PD II, OVC III & EN62109-1, PD II, OVC III
- Operating temperature is real ambient temperature around the driver core
- Environmental conditions see Technical Explanation

Characteristics					
Symbol	Conditions	min.	typ.	max.	Unit
$t_{\text{jitter(dig)}}$	Signal transfer deviation for digital filter selection <sup>10)</sup>		± 12.5		ns
$t_{\text{SPS(ana)}}$	Short pulse suppression for analog filter selection		0.2		µs
$t_{\text{SPS(dig)}}$	Short pulse suppression for digital filter selection		0.39		µs
$t_{\text{POR}}$	Power-on reset time		0.15		s
$t_{\text{reset}}$	Error reset time <sup>11)</sup>	0.03			ms
$V_{\text{CE(ref)}}$	Reference voltage for $V_{\text{CE}}$ -monitoring <sup>12)</sup>			9	V
$V_{\text{ITH(clamp)}}$	Input threshold voltage clamping (HIGH) <sup>13)</sup>			13	V
$V_{\text{ITL(clamp)}}$	Input threshold voltage clamping (LOW) <sup>13)</sup>	2			V
$R_{\text{IN(clamp)}}$	Input resistance (clamping inputs)		150		kΩ
$C_{\text{IN(clamp)}}$	Input capacitance (clamping inputs)			0.01	nF
$l_{\text{clear(PS)}}$	Shortest distance in air, primary side to secondary side	14			mm
$l_{\text{clear(SS)}}$	Shortest distance in air, secondary sides	6.1			mm
$l_{\text{creep(PS)}}$	Shortest distance along the surface, primary side to secondary side (CTI > 600)	15.1			mm
$l_{\text{creep(SS)}}$	Shortest distance along the surface, secondary sides (CTI > 600)	7.6			mm
$V_{\text{imp}}$	Impulse withstand voltage <sup>14)</sup>	12000			V
$V_{\text{PDPS}}$	Partial discharge extinction voltage, primary side to secondary side <sup>15)</sup>	2560			V
w	Weight		50		g
MTBF	Mean Time Between Failure <sup>16)</sup>		7.5		10 <sup>6</sup> h



## Footnotes

Footnote	Description
1)	The rated maximum output peak current is valid over the full operating temperature range. The maximum rated average output current will probably be limited by the operating temperature and the switching frequency. The derating factor has not been specified yet.
2)	The rated maximum switching frequency is limited by the operating temperature. The derating factor has not been specified yet.
3)	Repetitive peak voltage across the semiconductor power rails.
4)	The maximum DC-Link voltage is limited by creepage and clearance distances (according to EN61800-5-1, PD II, OVC III & EN62109-1, PD II, OVC III).
5)	Test Conditions: ACrms, 2s, input to output
6)	If using power semiconductor modules with gate charges $>2.5\mu\text{C}$ , the buffer capacitance of the driver's secondary sides and primary side has to be adjusted according to the corresponding Technical Explanation.
7)	Time between the driver detects an error at the secondary side until the primary side reports an error at the interface.
8)	Time between the driver receives an external error signal at the primary side until the driver turns off its outputs at the secondary side.
9)	The interlock dead time prevents the two outputs from being activated simultaneously. The dead time generation starts with each turn-off command at the driver's primary side. The interlock dead time generation could be deactivated via pin 'CFG_IDT'.
10)	The jitter is defined as the maximum deviation of the switching signal propagation delay time at constant environmental conditions. The signal transfer deviation $t_{\text{jitter(ana)}}$ is valid if analog filtering is selected via pin 'CFG_FLT' and the interlock dead time, generated by the controller, is longer than the interlock dead time which is ensured by the driver itself.
11)	Minimum time for which the driver is in error state.
12)	The driver detects a desaturation event, when one of its outputs is in on-state and the applied voltage at the corresponding $V_{\text{CE}}$ -monitoring input (pin 'VCE_IN') exceeds the reference voltage for $V_{\text{CE}}$ -monitoring. As long as the blanking time has not been elapsed, the desaturation detection is deactivated. The blanking time is adjustable via the 'CFG_VCE' pin.
13)	The driver's output switches to high-resistance state, when the output is in off-state and the applied voltage at the corresponding 'CLMP_IN' pin exceeds the input threshold voltage $V_{\text{ITH(clamp)}}$ . The output returns to off-state when the applied voltage at pin 'CLMP_IN' falls below the input threshold voltage $V_{\text{ITL(clamp)}}$ .
14)	Test condition: 12000V, pulse according to EN61800 & EN62109
15)	The partial discharge extinction voltage in this data sheet is defined as peak voltage.
16)	Conditions: $T_{\text{op}} = 40^{\circ}\text{C}$ ; full load
17)	All external circuits, except the $V_{\text{CE}}$ reference voltage adjustment, have to be supplied via pin 'PWR_VS_P_OUT' with respect to pin 'PWR_VS_N_OUT'. The rated average output current is reduced by the supply current of these external circuits.

## Pin description - primary side

PIN	Signal	Function	Specifications
X10:01	PWR_GND	Ground potential for power supply and digital signals	To be connected to ground
X10:02	CFG_IDT	Interlock dead time configuration	15V logic; 150kΩ (pull-up) LOW = 2μs interlock dead time HIGH = No interlock dead time
X10:03	nERR_OUT	Error output	Open collector output; max. 18V/15mA (external pull-up resistor needed) LOW = Error HIGH = No error
X10:04	nERR_IN	Error input	15V logic inverted; 150kΩ/10nF (pull-up) LOW = External error HIGH = No external error
X10:05	CFG_ERR	Error behavior configuration in case of secondary side error	15V logic; 150kΩ (pull-down) LOW = Both outputs switch off HIGH = Outputs switch off with next turn-off signal at the corresponding input
X10:06	CFG_FLT	Filter configuration for switching signals	15V logic; 150kΩ (pull-down) LOW = Analog filter ( $t_{SPS(ana)}$ ) HIGH = Digital filter ( $t_{SPS(dig)}$ )
X10:07	TOP_IN	Switching signal input (TOP)	15V logic; 33kΩ/0.01nF (pull-down) LOW = TOP switch off HIGH = TOP switch on
X10:08	BOT_IN	Switching signal input (BOT)	15V logic; 33kΩ/0.01nF (pull-down) LOW = BOT switch off HIGH = BOT switch on
X10:09	PWR_VS	Driver power supply	Stabilized +15V ±4%
X10:10	PWR_VS	Driver power supply	Stabilized +15V ±4%

## Pin description - secondary side - TOP

PIN	Signal	Function	Specifications
X100:01	CFG_VCE	V <sub>CE</sub> -monitoring reference voltage	External voltage divider needed
X100:02	VCE_IN	V <sub>CE</sub> -monitoring input	External blocking diode needed
X100:03	PWR_VS_P_OUT	Power supply output, positive voltage	Equal to V <sub>G(on)</sub> <sup>17</sup> (external buffer capacitors can be connected)
X100:04	nERR_IN	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X100:05	TOP_ON	On signal path to TOP semiconductor	External gate resistor needed (in consideration of I <sub>out(avg)</sub> , I <sub>out(peak)</sub> , V <sub>G(on)</sub> )
X100:06	TOP_OFF	Off signal path to TOP semiconductor	External gate resistor needed (in consideration of -I <sub>out(avg)</sub> , -I <sub>out(peak)</sub> , V <sub>G(off)</sub> )
X100:07	CLMP_IN	V <sub>CE</sub> -clamping input	150kΩ/0.01nF (pull-down) In case of activated TOP_OFF: LOW = TOP_OFF equal to V <sub>G(off)</sub> HIGH = TOP_OFF floating
X100:08	PWR_GND	Ground potential for power supply and digital signals	Reference potential for gate voltages (emitter/source of power semiconductor)
X100:09	TOP_SOFTOFF	SoftOff signal path to TOP semiconductor	External gate resistor needed
X100:10	PWR_VS_N_OUT	Power supply output, negative voltage	Equal to V <sub>G(off)</sub> <sup>17</sup> (external buffer capacitors can be connected)

## Pin description - secondary side - BOT

PIN	Signal	Function	Specifications
X200:01	CFG_VCE	V <sub>CE</sub> -monitoring reference voltage	External voltage divider needed
X200:02	VCE_IN	V <sub>CE</sub> -monitoring input	External blocking diode needed
X200:03	PWR_VS_P_OUT	Power supply output, positive voltage	Equal to V <sub>G(on)</sub> <sup>17)</sup> (external buffer capacitors can be connected)
X200:04	nERR_IN	External error input	15V logic inverted; 150kΩ/0.01nF (pull-up) LOW = External error HIGH = No external error
X200:05	BOT_ON	On signal path to BOT semiconductor	External gate resistor needed (in consideration of I <sub>out(avg)</sub> , I <sub>out(peak)</sub> , V <sub>G(on)</sub> )
X200:06	BOT_OFF	Off signal path to BOT semiconductor	External gate resistor needed (in consideration of -I <sub>out(avg)</sub> , -I <sub>out(peak)</sub> , V <sub>G(off)</sub> )
X200:07	CLMP_IN	V <sub>CE</sub> -clamping input	150kΩ/0.01nF (pull-down) In case of activated BOT_OFF: LOW = BOT_OFF equal to V <sub>G(off)</sub> HIGH = BOT_OFF floating
X200:08	PWR_GND	Ground potential for power supply and digital signals	Reference potential for gate voltages (emitter/source of power semiconductor)
X200:09	BOT_SOFTOFF	SoftOff signal path to BOT semiconductor	External gate resistor needed
X200:10	PWR_VS_N_OUT	Power supply output, negative voltage	Equal to V <sub>G(off)</sub> <sup>17)</sup> (external buffer capacitors can be connected)

This is an electrostatic discharge sensitive device (ESDS) due to international standard IEC 61340.

### \*IMPORTANT INFORMATION AND WARNINGS

The specifications of SEMIKRON products may not be considered as guarantee or assurance of product characteristics ("Beschaffenheitsgarantie"). The specifications of SEMIKRON products describe only the usual characteristics of products to be expected in typical applications, which may still vary depending on the specific application. Therefore, products must be tested for the respective application in advance. Application adjustments may be necessary. The user of SEMIKRON products is responsible for the safety of their applications embedding SEMIKRON products and must take adequate safety measures to prevent the applications from causing a physical injury, fire or other problem if any of SEMIKRON products become faulty. The user is responsible to make sure that the application design is compliant with all applicable laws, regulations, norms and standards. Except as otherwise explicitly approved by SEMIKRON in a written document signed by authorized representatives of SEMIKRON, SEMIKRON products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury. No representation or warranty is given and no liability is assumed with respect to the accuracy, completeness and/or use of any information herein, including without limitation, warranties of non-infringement of intellectual property rights of any third party. SEMIKRON does not assume any liability arising out of the applications or use of any product; neither does it convey any license under its patent rights, copyrights, trade secrets or other intellectual property rights, nor the rights of others. SEMIKRON makes no representation or warranty of non-infringement or alleged non-infringement of intellectual property rights of any third party which may arise from applications. Due to technical requirements our products may contain dangerous substances. For information on the types in question please contact the nearest SEMIKRON sales office. This document supersedes and replaces all information previously supplied and may be superseded by updates. SEMIKRON reserves the right to make changes.